XC4000-Series Features

Note: XC4000-Series devices described in this data sheet include the XC4000E, XC4000EX, XC4000L, and XC4000XL. This information does not apply to the older Xilinx families: XC4000, XC4000A, XC4000D or XC4000H. For information on these devices, see the Xilinx WEBLINX at http://www.xilinx.com.

- Third Generation Field-Programmable Gate Arrays
  - Select-RAM™ memory: on-chip ultra-fast RAM with
    - synchronous write option
    - dual-port RAM option
  - Fully PCI compliant (speed grades -3 and faster)
  - Abundant flip-flops
  - Flexible function generators
  - Dedicated high-speed carry logic
  - Wide edge decoders on each edge
  - Hierarchy of interconnect lines
  - Internal 3-state bus capability
  - 8 global low-skew clock or signal distribution networks
- System Performance to 66 MHz
- Flexible Array Architecture
- Systems-Oriented Features
  - IEEE 1149.1-compatible boundary scan logic support
  - Individually programmable output slew rate
  - Programmable input pull-up or pull-down resistors
  - 12-mA sink current per XC4000E output (4 mA per XC4000L output)
- Configured by Loading Binary File
  - Unlimited reprogrammability
- Readback Capability
- Backward Compatible with XC4000 Devices
- XACT*step* Development System runs on '386/'486/ Pentium-type PC, Sun-4, and Hewlett-Packard 700 series
  - Interfaces to popular design environments
  - Fully automatic mapping, placement and routing
  - Interactive design editor for design optimization
  - RAM/ROM compiler

Low-Voltage Versions Available

- Low-Voltage Devices Function at 3.0 - 3.6 Volts
- XC4000L: Low-Voltage Versions of XC4000E devices
- XC4000XL: Low-Voltage Versions of XC4000EX devices

Additional XC4000EX/XL Features

- Highest Capacity — Over 130,000 Usable Gates
- Additional Routing Over XC4000E
  - almost twice the routing capacity for high-density designs
- Buffered Interconnect for Maximum Speed
- New Latch Capability in Configurable Logic Blocks
- Improved VersaRing™ I/O Interconnect for Better Fixed Pinout Flexibility
- Flexible New High-Speed Clock Network
  - 8 additional Early Buffers for shorter clock delays
  - 4 additional FastCLK™ buffers for fastest clock input
  - Virtually unlimited number of clock signals
- Optional Multiplexer or 2-input Function Generator on Device Outputs
- High-Speed Parallel Express™ Configuration Mode
- Improved I/O Setup and Clock-to-Output with FastCLK and Global Early Buffers
- 4 Additional Address Bits in Master Parallel Configuration Mode

Introduction

XC4000-Series high-performance, high-capacity Field Programmable Gate Arrays (FPGAs) provide the benefits of custom CMOS VLSI, while avoiding the initial cost, long development cycle, and inherent risk of a conventional masked gate array.

The result of eleven years of FPGA design experience and feedback from thousands of customers, these FPGAs combine architectural versatility, on-chip Select-RAM memory with edge-triggered and dual-port modes, increased speed, abundant routing resources, and new, sophisticated software to achieve fully automated implementation of complex, high-density, high-performance designs.

The XC4000 Series currently has 19 members, as shown in Table 1.

Table 1: XC4000-Series Field Programmable Gate Arrays

Device	Max Logic Gates (No RAM)	Max. RAM Bits (No Logic)	Typical Gate Range (Logic and RAM)*	CLB Matrix	Total Logic Blocks	Number of Flip-Flops	Max. Decode Inputs per side	Max. User I/O
XC4003E	3,000	3,200	2,000 - 5,000	10 x 10	100	360	30	80
XC4005E/L	5,000	6,272	3,000 - 9,000	14 x 14	196	616	42	112
XC4006E	6,000	8,192	4,000 - 12,000	16 x 16	256	768	48	128
XC4008E	8,000	10,368	6,000 - 15,000	18 x 18	324	936	54	144
XC4010E/L	10,000	12,800	7,000 - 20,000	20 x 20	400	1,120	60	160
XC4013E/L	13,000	18,432	10,000 - 30,000	24 x 24	576	1,536	72	192
XC4020E	20,000	25,088	13,000 - 40,000	28 x 28	784	2,016	84	224
XC4025E	25,000	32,768	15,000 - 45,000	32 x 32	1,024	2,560	96	256
XC4028EX/XL	28,000	32,768	18,000 - 50,000	32 x 32	1,024	2,560	96	256
XC4036EX/XL	36,000	41,472	22,000 - 65,000	36 x 36	1,296	3,168	108	288
XC4044EX/XL	44,000	51,200	27,000 - 80,000	40 x 40	1,600	3,840	120	320
XC4052XL	52,000	61,952	33,000 - 100,000	44 x 44	1,936	4,576	132	352
XC4062XL	62,000	73,728	40,000 - 130,000	48 x 48	2,304	5,376	144	384
	Larger Devices Available in the First Half of 1997							

* Max values of Typical Gate Range include 20-30% of CLBs used as RAM.

Note: *Throughout the functional descriptions in this document, references to the XC4000E device family include the XC4000L, and references to the XC4000EX device family include the XC4000XL, unless explicitly stated otherwise. References to the XC4000 Series include the XC4000E, XC4000EX, XC4000L, and XC4000XL families. All functionality in low-voltage families is the same as in the corresponding 5-Volt family, except where numerical references are made to timing, power, or current-sinking capability.*

Description

XC4000-Series devices are implemented with a regular, flexible, programmable architecture of Configurable Logic Blocks (CLBs), interconnected by a powerful hierarchy of versatile routing resources, and surrounded by a perimeter of programmable Input/Output Blocks (IOBs). They have generous routing resources to accommodate the most complex interconnect patterns.

The devices are customized by loading configuration data into internal memory cells. The FPGA can either actively read its configuration data from an external serial or byte-parallel PROM (master modes), or the configuration data can be written into the FPGA from an external device (slave, peripheral and Express modes).

XC4000-Series FPGAs are supported by powerful and sophisticated software, covering every aspect of design from schematic or behavioral entry, floorplanning, simulation, automatic block placement and routing of interconnects, to the creation, downloading, and readback of the configuration bit stream.

Because Xilinx FPGAs can be reprogrammed an unlimited number of times, they can be used in innovative designs where hardware is changed dynamically, or where hardware must be adapted to different user applications. FPGAs are ideal for shortening design and development cycles, and also offer a cost-effective solution for production rates well beyond 5,000 systems per month. For lowest high-volume unit cost, a design can first be implemented in the XC4000E or XC4000EX, then migrated to one of Xilinx' compatible HardWire mask-programmed devices.

Table 2 shows density and performance for a few common circuit functions that can be implemented in XC4000-Series devices.

Table 2: Density and Performance for Several Common Circuit Functions in XC4000E[1]

Design Class	Function	CLBs Used	XC4000E-3	XC4000E-2	Units
Memory	256 x 8 Single Port (read/modify/write)	72	63	80	MHz
	32 x 16 bit FIFO				
	simultaneous read/write	48	63	80	MHz
	MUXed read/write	32	63	80	MHz
Logic	9 bit Shift Register (with enable)	5	170	200	MHz
	16 bit Pre-Scaled Counter	8	142	170	MHz
	16 bit Loadable Counter	8	65	76	MHz
	16 bit Accumulator	9	65	76	MHz
	8 bit, 16 tap FIR Filter sample rate				
	parallel	400	55	65	MHz
	serial	68	8.1	10	MHz
	8 x 8 Parallel Multiplier				
	single stage, register to register	73	37	30	ns
	16 bit Address Decoder (internal decode)	3	4.7	3.9	ns
	9 bit Parity Checker	1	4.3	2.7	ns

Note: 1. Most functions are faster in XC4000EX due to faster carry logic, direct connects, and other additional interconnect.

Taking Advantage of Reconfiguration

FPGA devices can be reconfigured to change logic function while resident in the system. This capability gives the system designer a new degree of freedom not available with any other type of logic.

Hardware can be changed as easily as software. Design updates or modifications are easy, and can be made to products already in the field. An FPGA can even be reconfigured dynamically to perform different functions at different times.

Reconfigurable logic can be used to implement system self-diagnostics, create systems capable of being reconfigured for different environments or operations, or implement multi-purpose hardware for a given application. As an added benefit, using reconfigurable FPGA devices simplifies hardware design and debugging and shortens product time-to-market.

XC4000E and XC4000EX Families Compared to the XC4000

For readers already familiar with the XC4000 family of Xilinx Field Programmable Gate Arrays, the major new features in the XC4000-Series devices are listed in this section. The biggest advantages of XC4000E and XC4000EX devices are significantly increased system speed, greater capacity, and new architectural features, particularly Select-RAM memory. The XC4000EX devices also offer many new routing features, including special high-speed clock buffers that can be used to capture input data with minimal delay.

Any XC4000E device is pinout- and bitstream-compatible with the corresponding XC4000 device. An existing XC4000 bitstream can be used to program an XC4000E device. However, since the XC4000E includes many new features, an XC4000E bitstream cannot be loaded into an XC4000 device.

Most XC4000EX devices have no corresponding XC4000 devices, because of the larger CLB arrays. The XC4028EX has the same array size as the XC4025 and XC4025E, but is not bitstream-compatible. However, the XC4025, XC4025E, and XC4028EX are all pinout-compatible.

Improvements in XC4000E and XC4000EX

Increased System Speed

Delays in FPGA-based designs are layout dependent. There is a rule of thumb designers can consider—the system clock rate should not exceed one third to one half of the specified toggle rate. Critical portions of a design, such as shift registers and simple counters, can run faster—approximately two thirds of the specified toggle rate.

XC4000E and XC4000EX devices can run at synchronous system clock rates of up to 66 MHz, and internal performance can exceed 150 MHz. This increase in performance over the previous families stems from improvements in both device processing and system architecture. XC4000-Series devices use a sub-micron triple-layer metal process. In addition, many architectural improvements have been made, as described below.

PCI Compliance

XC4000-Series -3 and faster speed grades are fully PCI compliant. XC4000E and XC4000EX devices can be used to implement a one-chip PCI solution.

Carry Logic

The speed of the carry logic chain has increased dramatically. Some parameters, such as the delay on the carry chain through a single CLB (TBYP), have improved by as much as 50% from XC4000 values. See "Fast Carry Logic" on page 21 for more information.

Select-RAM Memory: Edge-Triggered, Synchronous RAM Modes

The RAM in any CLB can be configured for synchronous, edge-triggered, write operation. The read operation is not affected by this change to an edge-triggered write.

Dual-Port RAM

A separate option converts the 16x2 RAM in any CLB into a 16x1 dual-port RAM with simultaneous Read/Write.

The function generators in each CLB can be configured as either level-sensitive (asynchronous) single-port RAM, edge-triggered (synchronous) single-port RAM, edge-triggered (synchronous) dual-port RAM, or as combinatorial logic.

Configurable RAM Content

The RAM content can now be loaded at configuration time, so that the RAM starts up with user-defined data.

H Function Generator

In XC4000-Series devices, the H function generator is more versatile than in the XC4000. Its inputs can come not only from the F and G function generators but also from up to three of the four control input lines. The H function generator can thus be totally or partially independent of the other two function generators, increasing the maximum capacity of the device.

IOB Clock Enable

The two flip-flops in each IOB have a common clock enable input, which through configuration can be activated individually for the input or output flip-flop or both. This clock enable operates exactly like the EC pin on the XC4000 CLB. This new feature makes the IOBs more versatile, and avoids the need for clock gating.

Output Drivers

The output pull-up structure defaults to a TTL-like totem-pole. This driver is an n-channel pull-up transistor, pulling to a voltage one transistor threshold below Vcc, just like the XC4000 outputs. Alternatively, XC4000-Series devices can be globally configured with CMOS outputs, with p-channel pull-up transistors pulling to Vcc. Also, the configurable pull-up resistor in the XC4000 Series is a p-channel transistor that pulls to Vcc, whereas in the XC4000 it is an n-channel transistor that pulls to a voltage one transistor threshold below Vcc.

Input Thresholds

The input thresholds can be globally configured for either TTL (1.2 V threshold) or CMOS (2.5 V threshold), just like XC2000 and XC3000 inputs. The two global adjustments of input threshold and output level are independent of each other.

Global Signal Access to Logic

There is additional access from global clocks to the F and G function generator inputs.

Configuration Pin Pull-Up Resistors

During configuration, the three mode pins, M0, M1, and M2, have weak pull-up resistors. For the most popular configuration mode, Slave Serial, the mode pins can thus be left unconnected.

The three mode inputs can be individually configured with or without weak pull-up or pull-down resistors after configuration.

The $\overline{\text{PROGRAM}}$ input pin has a permanent weak pull-up.

Soft Start-up

Like the XC3000A, XC4000-Series devices have "Soft Start-up." When the configuration process is finished and the device starts up, the first activation of the outputs is automatically slew-rate limited. This feature avoids potential ground bounce when all outputs are turned on simultaneously. Immediately after start-up, the slew rate of the individual outputs is, as in the XC4000 family, determined by the individual configuration option.

XC4000 and XC4000A Compatibility

Existing XC4000 bitstreams can be used to configure an XC4000E device. XC4000A bitstreams must be recompiled for use with the XC4000E due to improved routing resources, although the devices are pin-for-pin compatible.

Additional Improvements in XC4000EX Only

Increased Routing

New interconnect in the XC4000EX includes twenty-two additional vertical lines in each column of CLBs and twelve new horizontal lines in each row of CLBs. The twelve "Quad Lines" in each CLB row and column include optional repowering buffers for maximum speed. Additional high-performance routing near the IOBs enhances pin flexibility.

Faster Input and Output

A fast, dedicated early clock sourced by global clock buffers is available for the IOBs. To ensure synchronization with the regular global clocks, a Fast Capture latch driven by the early clock is available. The input data can be initially loaded into the Fast Capture latch with the early clock, then transferred to the input flip-flop or latch with the low-skew global clock. A programmable delay on the input can be used to avoid hold-time requirements. See "IOB Input Signals" on page 24 for more information.

Latch Capability in CLBs

Storage elements in the XC4000EX CLB can be configured as either flip-flops or latches. This capability makes the FPGA highly synthesis-compatible.

IOB Output MUX From Output Clock

A multiplexer in the IOB allows the output clock to select either the output data or the IOB clock enable as the output to the pad. Thus, two different data signals can share a single output pad, effectively doubling the number of device outputs without requiring a larger, more expensive package. This multiplexer can also be configured as an AND-gate to implement a very fast pin-to-pin path. See "IOB Output Signals" on page 27 for more information.

Express Configuration Mode

A new slave configuration mode accepts parallel data input. Data is processed in parallel, rather than serialized internally. Therefore, the data rate is eight times that of the six conventional configuration modes.

Additional Address Bits

Larger devices require more bits of configuration data. A daisy chain of several large XC4000EX devices may require a PROM that cannot be addressed by the eighteen address bits supported in the XC4000E. The XC4000EX family therefore extends the addressing in Master Parallel configuration mode to 22 bits.

Table 3: CLB Count of Selected XC4000-Series Soft Macros

7400 Equivalents	CLBs
'138	5
'139	2
'147	5
'148	6
'150	5
'151	3
'152	3
'153	2
'154	16
'157	2
'158	2
'160	5
'161	6
'162	8
'163	8
'164	4
'165s	9
'166	5
'168	7
'174	3
'194	5
'195	3
'280	3
'283	8
'298	2
'352	2
'390	3
'518	3
'521	3

Explanation of RAM nomenclature
- s = single-port edge-triggered
- d = dual-port edge-triggered
- no extension = level-sensitive

Barrel Shifters	CLBs
brlshft4	4
brlshft8	13
4-Bit Counters	
cd4cd	3
cd4cle	5
cd4rle	6
cb4ce	3
cb4cle	6
cb4re	5
8- and 16-Bit Counters	
cb8ce	6
cb8re	10
cc16ce	9
cc16cle	9
cc16cled	21
Identity Comparators	
comp4	1
comp8	2
comp16	5
Magnitude Comparators	
compm4	4
compm8	9
compm16	20

RAMs	
ram16x4	2
ram16x4s	2
ram16x4d	4

Multiplexers	CLBs
m2-1e	1
m4-1e	1
m8-1e	3
m16-1e	5
Registers	
rd4r	2
rd8r	4
rd16r	8
Shift Registers	
sr8ce	4
sr16re	8
Decoders	
d2-4e	2
d3-8e	4
d4-16e	16

Explanation of counter nomenclature
- cb = binary counter
- cd = BCD counter
- cc = cascadable binary counter
- d = bidirectional
- l = loadable
- e = clock enable
- r = synchronous reset
- c = asynchronous clear

Detailed Functional Description

XC4000-Series devices achieve high speed through advanced semiconductor technology and improved architecture. The XC4000E and XC4000EX support system clock rates of up to 66 MHz and internal performance in excess of 150 MHz. Compared to older Xilinx FPGA families, XC4000-Series devices are more powerful. They offer on-chip edge-triggered and dual-port RAM, clock enables on I/O flip-flops, and wide-input decoders. They are more versatile in many applications, especially those involving RAM. Design cycles are faster due to a combination of increased routing resources and more sophisticated software.

Basic Building Blocks

Xilinx user-programmable gate arrays include two major configurable elements: configurable logic blocks (CLBs) and input/output blocks (IOBs).

- CLBs provide the functional elements for constructing the user's logic.
- IOBs provide the interface between the package pins and internal signal lines.

Three other types of circuits are also available:

- 3-State buffers (TBUFs) driving horizontal longlines are associated with each CLB.
- Wide edge decoders are available around the periphery of each device.
- An on-chip oscillator is provided.

Programmable interconnect resources provide routing paths to connect the inputs and outputs of these configurable elements to the appropriate networks.

The functionality of each circuit block is customized during configuration by programming internal static memory cells. The values stored in these memory cells determine the logic functions and interconnections implemented in the FPGA.

Each of these available circuits is described in this section.

Configurable Logic Blocks (CLBs)

Configurable Logic Blocks implement most of the logic in an FPGA. The principal CLB elements are shown in Figure 1. The number of CLBs needed to implement selected soft macros is shown in Table 3.

Two 4-input function generators (F and G) offer unrestricted versatility. Most combinatorial logic functions need four or fewer inputs. However, a third function generator (H) is provided. The H function generator has three inputs. Either zero, one, or both of these inputs can be the outputs of F and G; the other input(s) are from outside the CLB. The CLB can, therefore, implement certain functions of up to nine variables, like parity check or expandable-identity comparison of two sets of four inputs.

Each CLB contains two storage elements that can be used to store the function generator outputs. However, the storage elements and function generators can also be used independently. These storage elements can be configured as flip-flops in both XC4000E and XC4000EX devices; in the XC4000EX they can optionally be configured as latches. DIN can be used as a direct input to either of the two storage elements. H1 can drive the other through the H function generator. Function generator outputs can also drive two outputs independent of the storage element outputs. This versatility increases logic capacity and simplifies routing.

Thirteen CLB inputs and four CLB outputs provide access to the function generators and storage elements. These inputs and outputs connect to the programmable interconnect resources outside the block.

Function Generators

Four independent inputs are provided to each of two function generators (F1 - F4 and G1 - G4). These function generators, with outputs labeled F' and G', are each capable of implementing any arbitrarily defined Boolean function of four inputs. The function generators are implemented as memory look-up tables. The propagation delay is therefore independent of the function implemented.

A third function generator, labeled H', can implement any Boolean function of its three inputs. Two of these inputs can optionally be the F' and G' functional generator outputs. Alternatively, one or both of these inputs can come from outside the CLB (H2, H0). The third input must come from outside the block (H1).

Signals from the function generators can exit the CLB on two outputs. F' or H' can be connected to the X output. G' or H' can be connected to the Y output.

A CLB can be used to implement any of the following functions:

- any function of up to four variables, plus any second function of up to four unrelated variables, plus any third function of up to three unrelated variables[1]
- any single function of five variables
- any function of four variables together with some functions of six variables
- some functions of up to nine variables.

1. When three separate functions are generated, one of the function outputs must be captured in a flip-flop internal to the CLB. Only two unregistered function generator outputs are available from the CLB.

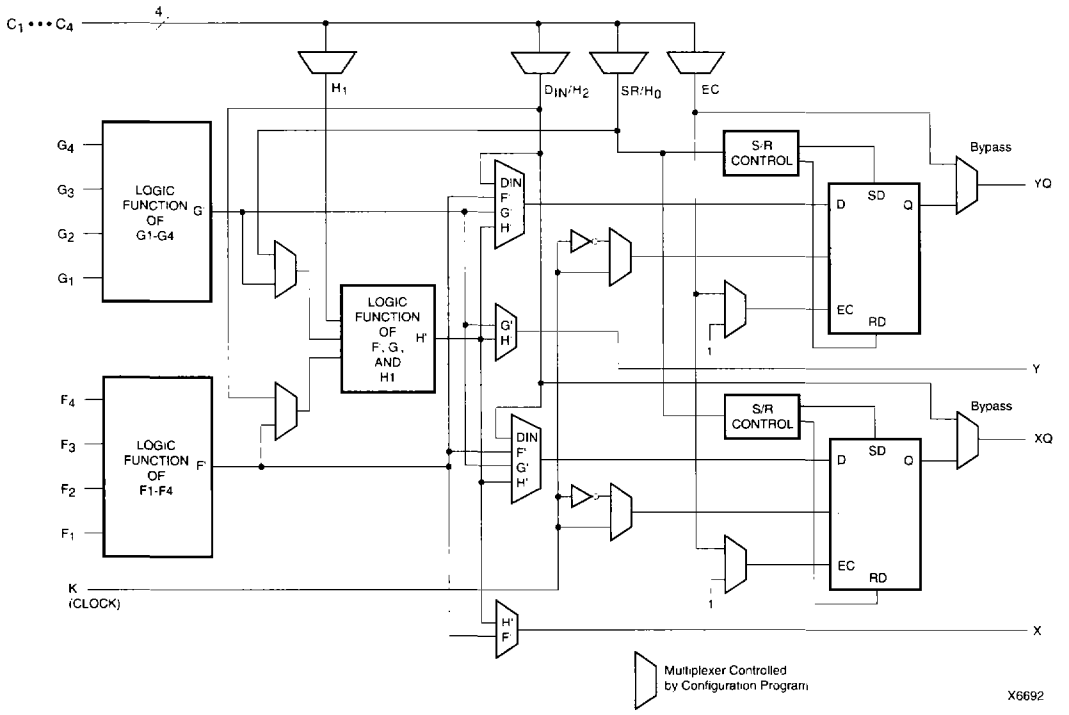


Figure 1: Simplified Block Diagram of XC4000-Series CLB (RAM and Carry Logic functions not shown)

Implementing wide functions in a single block reduces both the number of blocks required and the delay in the signal path, achieving both increased capacity and speed.

The versatility of the CLB function generators significantly improves system speed. In addition, the design-software tools can deal with each function generator independently. This flexibility improves cell usage.

Flip-Flops

The CLB can pass the combinatorial output(s) to the interconnect network, but can also store the combinatorial results or other incoming data in one or two flip-flops, and connect their outputs to the interconnect network as well.

The two edge-triggered D-type flip-flops have common clock (K) and clock enable (EC) inputs. Either or both clock inputs can also be permanently enabled. Storage element functionality is described in Table 4.

Latches (XC4000EX only)

The CLB storage elements can also be configured as latches. The two latches have common clock (K) and clock enable (EC) inputs. Storage element functionality is described in Table 4.

Table 4: CLB Storage Element Functionality (active rising edge is shown)

Mode	K	EC	SR	D	Q
Power-Up or GSR	X	X	X	X	SR
Flip-Flop	X	X	1	X	SR
	⎍⎍	1*	0*	D	D
	0	X	0*	X	Q
Latch	1	1*	0*	X	Q
	0	1*	0*	D	D
Both	X	0	0*	X	Q

Legend:

X	Don't care
⎍⎍	Rising edge
SR	Set or Reset value. Reset is default.
0*	Input is Low or unconnected (default value)
1*	Input is High or unconnected (default value)

Clock Input

Each flip-flop can be triggered on either the rising or falling clock edge. The clock pin is shared by both storage elements. However, the clock is individually invertible for each storage element. Any inverter placed on the clock input is automatically absorbed into the CLB.

Clock Enable

The clock enable signal (EC) is active High. The EC pin is shared by both storage elements. If left unconnected for either, the clock enable for that storage element defaults to the active state. EC is not invertible within the CLB.

Set/Reset

An asynchronous storage element input (SR) can be configured as either set or reset. This configuration option determines the state in which each flip-flop becomes operational after configuration. It also determines the effect of a Global Set/Reset pulse during normal operation, and the effect of a pulse on the SR pin of the CLB. All three set/reset functions for any single flip-flop are controlled by the same configuration data bit.

The set/reset state can be independently specified for each flip-flop. This input can also be independently disabled for either flip-flop.

The set/reset state is specified by using the INIT attribute, or by placing the appropriate set or reset flip-flop library symbol.

SR is active High. It is not invertible within the CLB.

Global Set/Reset

A separate Global Set/Reset line (not shown in Figure 1) sets or clears each storage element during power-up, reconfiguration, or when a dedicated Reset net is driven active. This global net (GSR) does not compete with other routing resources; it uses a dedicated distribution network.

Each flip-flop is configured as either globally set or reset in the same way that the local set/reset (SR) is specified. Therefore, if a flip-flop is set by SR, it is also set by GSR. Similarly, a reset flip-flop is reset by both SR and GSR.

GSR can be driven from any user-programmable pin as a global reset input. To use this global net, place an input pad and input buffer in the schematic or HDL code, driving the GSR pin of the STARTUP symbol. (See Figure 2.) A specific pin location can be assigned to this input using a LOC attribute or property, just as with any other user-programmable pad. An inverter can optionally be inserted after the input buffer to invert the sense of the Global Set/Reset signal.

Alternatively, GSR can be driven from any internal node.

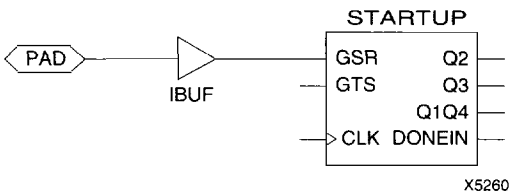


Figure 2: Schematic Symbols for Global Set/Reset

Data Inputs and Outputs

The source of a storage element data input is programmable. It is driven by any of the functions F', G', and H', or by the Direct In (DIN) block input. The flip-flops or latches drive the XQ and YQ CLB outputs.

Two fast feed-through paths are available, as shown in Figure 1. A two-to-one multiplexer on each of the XQ and YQ outputs selects between a storage element output and any of the control inputs. This bypass is sometimes used by the automated router to repower internal signals.

Control Signals

Multiplexers in the CLB map the four control inputs (C1 - C4 in Figure 1) into the four internal control signals (H1, DIN/H2, SR/H0, and EC). Any of these inputs can drive any of the four internal control signals.

When the logic function is enabled, the four inputs are:

- EC — Enable Clock
- SR/H0 — Asynchronous Set/Reset or H function generator Input 0
- DIN/H2 — Direct In or H function generator Input 2
- H1 — H function generator Input 1.

When the memory function is enabled, the four inputs are:

- EC — Enable Clock
- WE — Write Enable
- D0 — Data Input to F and/or G function generator
- D1 — Data input to G function generator (16x1 and 16x2 modes) or 5th Address bit (32x1 mode).

Using FPGA Flip-Flops and Latches

The abundance of flip-flops in the XC4000 Series invites pipelined designs. This is a powerful way of increasing performance by breaking the function into smaller subfunctions and executing them in parallel, passing on the results through pipeline flip-flops. This method should be seriously considered wherever throughput is more important than latency.

To include a CLB flip-flop, place the appropriate library symbol. For example, FDCE is a D-type flip-flop with clock enable and asynchronous clear. The corresponding latch symbol (for the XC4000EX only) is called LDCE.

In XC4000-Series devices, the flip flops can be used as registers or shift registers without blocking the function generators from performing a different, perhaps unrelated task. This ability increases the functional capacity of the devices.

The CLB setup time is specified between the function generator inputs and the clock input K. Therefore, the specified CLB flip-flop setup time includes the delay through the function generator.

Using Function Generators as RAM

Optional modes for each CLB make the memory look-up tables in the F' and G' function generators usable as an array of Read/Write memory cells. Available modes are level-sensitive (similar to the XC4000/A/H families), edge-triggered, and dual-port edge-triggered. Depending on the selected mode. a single CLB can be configured as either a 16x2. 32x1, or 16x1 bit array.

Supported CLB memory configurations and timing modes for single- and dual-port modes are shown in Table 5.

XC4000-Series devices are the first programmable logic devices with edge-triggered (synchronous) and dual-port RAM accessible to the user. Edge-triggered RAM simplifies system timing. Dual-port RAM doubles the effective throughput of FIFO applications. These features can be individually programmed in any XC4000-Series CLB.

Advantages of On-Chip and Edge-Triggered RAM

The on-chip RAM is extremely fast. The read access time is the same as the logic delay. The write access time is slightly slower. Both access times are much faster than any off-chip solution, because they avoid I/O delays.

Edge-triggered RAM, also called synchronous RAM, is a feature never before available in a Field Programmable Gate Array. The simplicity of designing with edge-triggered RAM, and the markedly higher achievable performance, add up to a significant improvement over existing devices with on-chip RAM.

Three application notes are available from Xilinx that discuss edge-triggered RAM: "*XC4000E Edge-Triggered and Dual-Port RAM Capability*," "*Implementing FIFOs in XC4000E RAM*," and "*Synchronous and Asynchronous FIFO Designs*." All three application notes apply to both XC4000E and XC4000EX RAM.

Table 5: Supported RAM Modes

	16 x 1	16 x 2	32 x 1	Edge-Triggered Timing	Level-Sensitive Timing
Single-Port	√	√	√	√	√
Dual-Port	√			√	

RAM Configuration Options

The function generators in any CLB can be configured as RAM arrays in the following sizes:

- Two 16x1 RAMs: two data inputs and two data outputs with identical or, if preferred, different addressing for each RAM
- One 32x1 RAM: one data input and one data output.

One F or G function generator can be configured as a 16x1 RAM while the other function generators are used to implement any function of up to 5 inputs.

Additionally, the XC4000-Series RAM may have either of two timing modes:

- Edge-Triggered (Synchronous): data written by the designated edge of the CLB clock. WE acts as a true clock enable.
- Level-Sensitive (Asynchronous): an external WE signal acts as the write strobe.

The selected timing mode applies to both function generators within a CLB when both are configured as RAM.

The number of read ports is also programmable:

- Single Port: each function generator has a common read and write port
- Dual Port: both function generators are configured together as a single 16x1 dual-port RAM with one write port and two read ports. Simultaneous read and write operations to the same or different addresses are supported.

RAM configuration options are selected by placing the appropriate library symbol.

Choosing a RAM Configuration Mode

The appropriate choice of RAM mode for a given design should be based on timing and resource requirements, desired functionality, and the simplicity of the design process. Recommended usage is shown in Table 6.

The difference between level-sensitive, edge-triggered, and dual-port RAM is only in the write operation. Read operation and timing is identical for all modes of operation.

Table 6: RAM Mode Selection

	Level-Sensitive	Edge-Triggered	Dual-Port Edge-Triggered
Use for New Designs?	No	Yes	Yes
Size (16x1, Registered)	1/2 CLB	1/2 CLB	1 CLB
Simultaneous Read/Write	No	No	Yes
Relative Performance	X	2X	2X (4X effective)

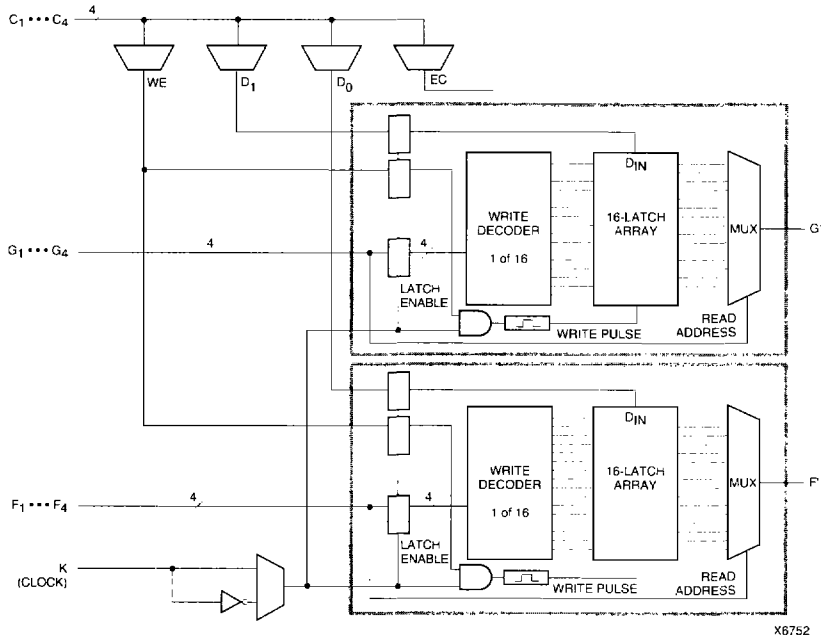


Figure 3: 16x2 (or 16x1) Edge-Triggered Single-Port RAM

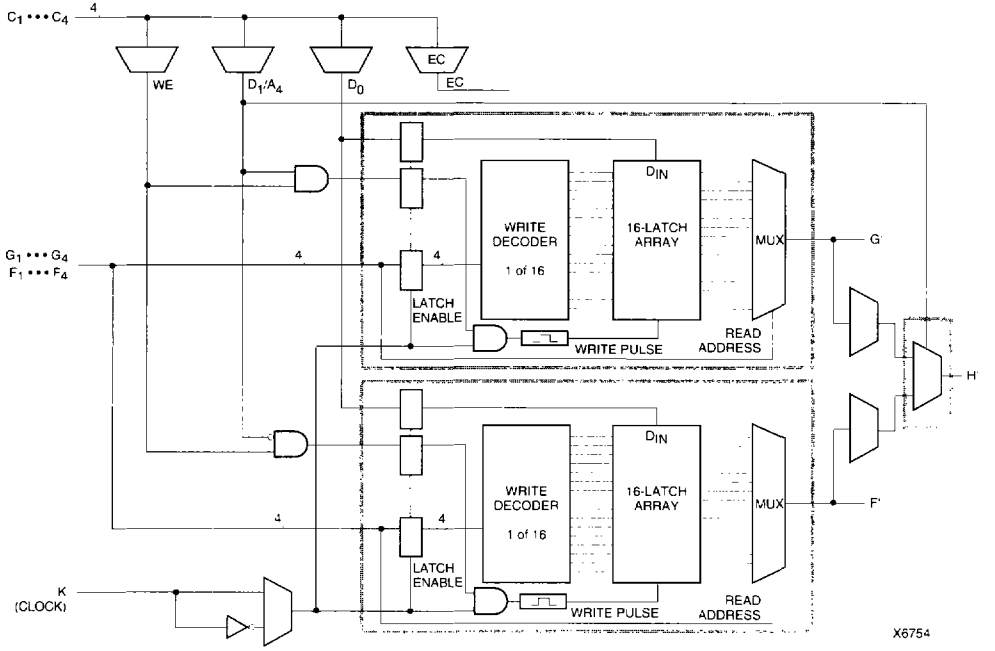


Figure 4: 32x1 Edge-Triggered Single-Port RAM (F and G addresses are identical)

RAM Inputs and Outputs

The F1-F4 and G1-G4 inputs to the function generators act as address lines, selecting a particular memory cell in each look-up table.

The functionality of the CLB control signals changes when the function generators are configured as RAM. The DIN/H2, H1, and SR/H0 lines become the two data inputs (D0, D1) and the Write Enable (WE) input for the 16x2 memory. When the 32x1 configuration is selected, D1 acts as the fifth address bit and D0 is the data input.

The contents of the memory cell(s) being addressed are available at the F' and G' function-generator outputs. They can exit the CLB through its X and Y outputs, or can be captured in the CLB flip-flop(s).

Configuring the CLB function generators as Read/Write memory does not affect the functionality of the other portions of the CLB, with the exception of the redefinition of the control signals. In 16x2 and 16x1 modes, the H' function generator can be used to implement Boolean functions of F', G', and D1, and the D flip-flops can latch the F', G', H', or D0 signals.

Single-Port Edge-Triggered Mode

Edge-triggered (synchronous) RAM simplifies timing requirements. XC4000-Series edge-triggered RAM timing operates like writing to a data register. Data and address are presented. The register is enabled for writing by a logic High on the write enable input, WE. Then a rising or falling clock edge loads the data into the register, as shown in Figure 5.

Complex timing relationships between address, data, and write enable signals are not required, and the external write enable pulse becomes a simple clock enable. The active edge of WCLK latches the address, input data, and WE signals. An internal write pulse is generated that performs the write. See Figure 3 and Figure 4 for block diagrams of a CLB configured as 16x2 and 32x1 edge-triggered, single-port RAM.

The relationships between CLB pins and RAM inputs and outputs for single-port, edge-triggered mode are shown in Table 7.

The Write Clock input (WCLK) can be configured as active on either the rising edge (default) or the falling edge. It uses the same CLB pin (K) used to clock the CLB flip-flops, but it can be independently inverted. Consequently, the RAM output can optionally be registered within the same

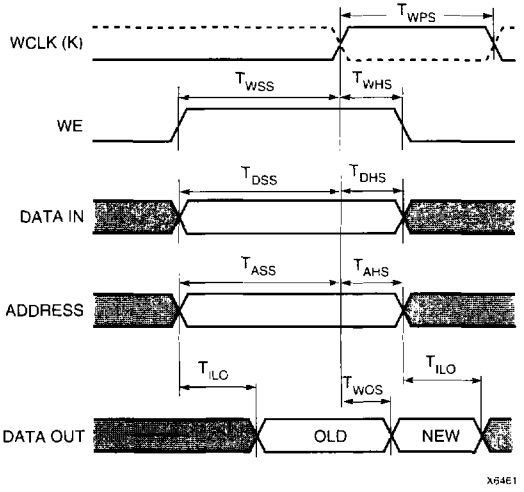


Figure 5: Edge-Triggered RAM Write Timing

CLB either by the same clock edge as the RAM, or by the opposite edge of this clock. The sense of WCLK applies to both function generators in the CLB when both are configured as RAM.

The WE pin is active-High and is not invertible within the CLB.

Note: The pulse following the active edge of WCLK (T_{WPS} in Figure 5) must be less than one millisecond wide. For most applications, this requirement is not overly restrictive; *however, it must not be forgotten. Stopping WCLK at this* point in the write cycle could result in excessive current and even damage to the larger devices if many CLBs are configured as edge-triggered RAM.

Table 7: Single-Port Edge-Triggered RAM Signals

RAM Signal	CLB Pin	Function
D	D0 or D1 (16x2, 16x1) D0 (32x1)	Data In
A[3:0]	F1-F4 or G1-G4	Address
A[4]	D1 (32x1)	Address
WE	WE	Write Enable
WCLK	K	Clock
SPO (Data Out)	F' or G'	Single Port Out (Data Out)

Dual-Port Edge-Triggered Mode

In dual-port mode, both the F and G function generators are used to create a single 16x1 RAM array with one write port and two read ports. The resulting RAM array can be read and written simultaneously at two independent addresses. Simultaneous read and write operations at the same address are also supported.

Dual-port mode always has edge-triggered write timing, as shown in Figure 5.

Figure 6 shows a simple model of an XC4000-Series CLB configured as dual-port RAM. One address port, labeled A[3:0], supplies both the read and write address for the F function generator. This function generator behaves the same as a 16x1 single-port edge-triggered RAM array. The RAM output, Single Port Out (SPO), appears at the F function generator output. SPO, therefore, reflects the data at address A[3:0].

The other address port, labeled DPRA[3:0] for Dual Port Read Address, supplies the read address for the G function generator. The write address for the G function generator, however, comes from the address A[3:0]. The output from this 16x1 RAM array, Dual Port Out (DPO), appears at the G function generator output. DPO, therefore, reflects the data at address DPRA[3:0].

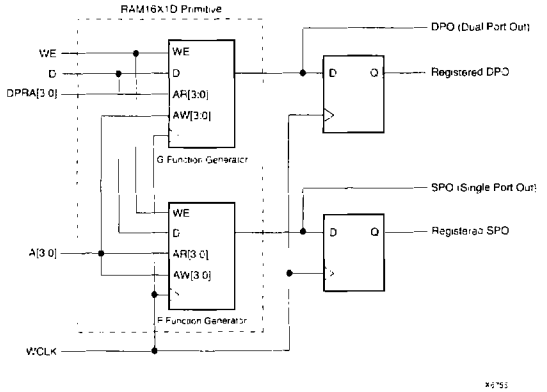


Figure 6: XC4000-Series Dual-Port RAM, Simple Model

Therefore, by using A[3:0] for the write address and DPRA[3:0] for the read address, and reading only the DPO output, a FIFO that can read and write simultaneously is easily generated. Simultaneous access doubles the effective throughput of the FIFO.

The relationships between CLB pins and RAM inputs and outputs for dual-port, edge-triggered mode are shown in Table 8. See Figure 7 for a block diagram of a CLB configured in this mode.

Note: The pulse following the active edge of WCLK (T_{WPS} in Figure 5) must be less than one millisecond wide. For most applications, this requirement is not overly restrictive; however, it must not be forgotten. Stopping WCLK at this point in the write cycle could result in excessive current and even damage to the larger devices if many CLBs are configured as edge-triggered RAM.

Table 8: Dual-Port Edge-Triggered RAM Signals

RAM Signal	CLB Pin	Function
D	D0	Data In
A[3:0]	F1-F4	Read Address for F, Write Address for F and G
DPRA[3:0]	G1-G4	Read Address for G
WE	WE	Write Enable
WCLK	K	Clock
SPO	F'	Single Port Out (addressed by A[3:0])
DPO	G'	Dual Port Out (addressed by DPRA[3:0])

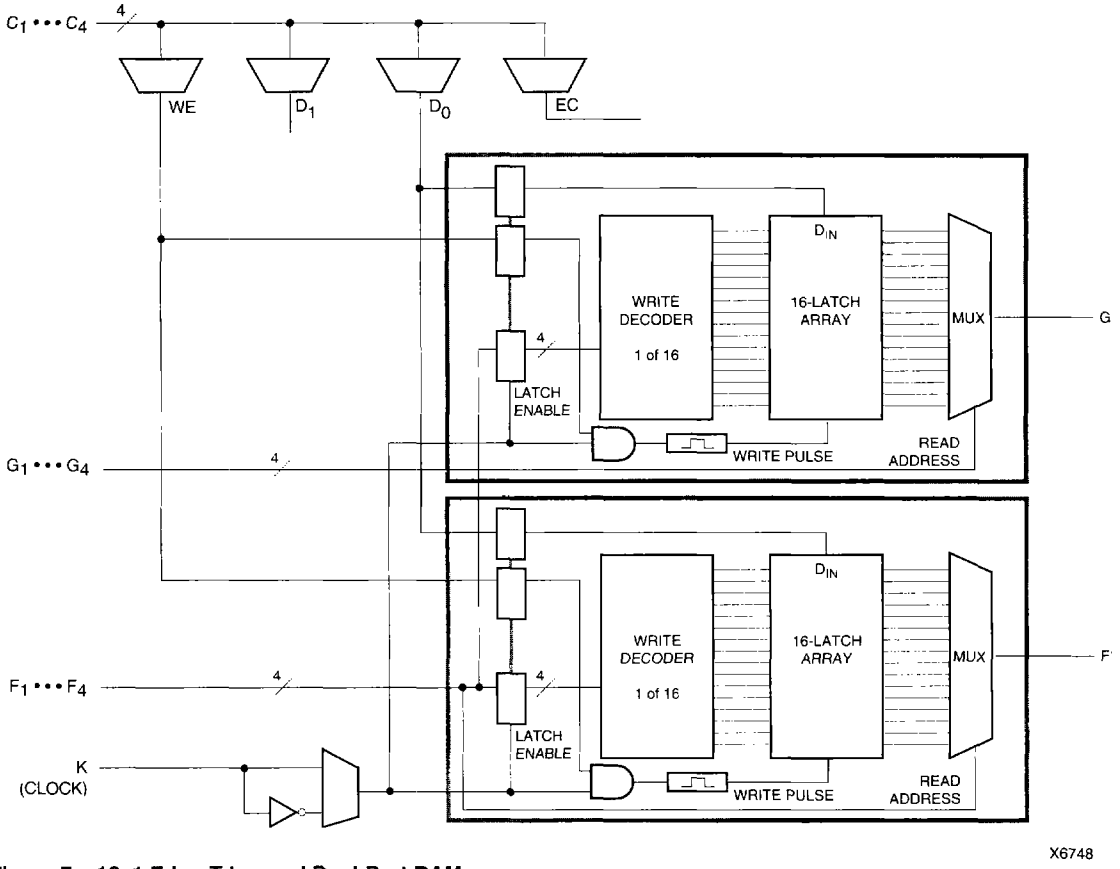


Figure 7: 16x1 Edge-Triggered Dual-Port RAM

Single-Port Level-Sensitive Timing Mode

Note: Edge-triggered mode is recommended for all new designs. Level-sensitive mode, also called asynchronous mode, is still supported for XC4000-Series backward-compatibility with the XC4000 family.

Level-sensitive RAM timing is simple in concept but can be complicated in execution. Data and address signals are presented, then a positive pulse on the write enable pin (WE) performs a write into the RAM at the designated address. As indicated by the "level-sensitive" label, this RAM acts like a latch. During the WE High pulse, changing the data lines results in new data written to the old address. Changing the address lines while WE is High results in spurious data written to the new address—and possibly at other addresses as well, as the address lines inevitably do not all change simultaneously.

The user must generate a carefully timed WE signal. The delay on the WE signal and the address lines must be carefully verified to ensure that WE does not become active until after the address lines have settled, and that WE goes inactive before the address lines change again. The data must be stable before and after the falling edge of WE.

In practical terms, WE is usually generated by a 2X clock. If a 2X clock is not available, the falling edge of the system clock can be used. However, there are inherent risks in this approach, since the WE pulse must be guaranteed inactive before the next rising edge of the system clock. Several older application notes are available from Xilinx that discuss the design of level-sensitive RAMs. These application notes include XAPP031, "*Using the XC4000 RAM Capability*" and XAPP042, "*High-Speed RAM Design in XC4000*."

However, the edge-triggered RAM available in the XC4000 Series is superior to level-sensitive RAM for almost every application.

Figure 8 shows the write timing for level-sensitive, single-port RAM.

The relationships between CLB pins and RAM inputs and outputs for single-port level-sensitive mode are shown in Table 9.

Figure 9 and Figure 10 show block diagrams of a CLB configured as 16x2 and 32x1 level-sensitive, single-port RAM.

Initializing RAM at Configuration

Both RAM and ROM implementations of the XC4000-Series devices are initialized during configuration. The initial contents are defined via an INIT attribute or property attached to the RAM or ROM symbol, as described in the schematic library guide.

If not defined, all RAM contents are initialized to all zeros, by default.

RAM initialization occurs only during configuration. The RAM content is not affected by Global Set/Reset.

Table 9: Single-Port Level-Sensitive RAM Signals

RAM Signal	CLB Pin	Function
D	D0 or D1	Data In
A[3:0]	F1-F4 or G1-G4	Address
WE	WE	Write Enable
O	F' or G'	Data Out

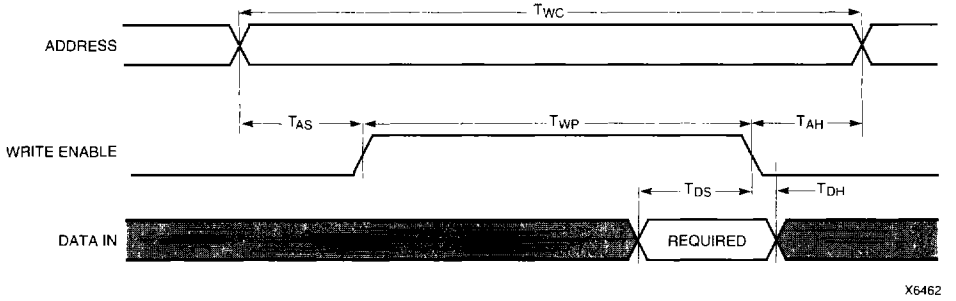


Figure 8: Level-Sensitive RAM Write Timing

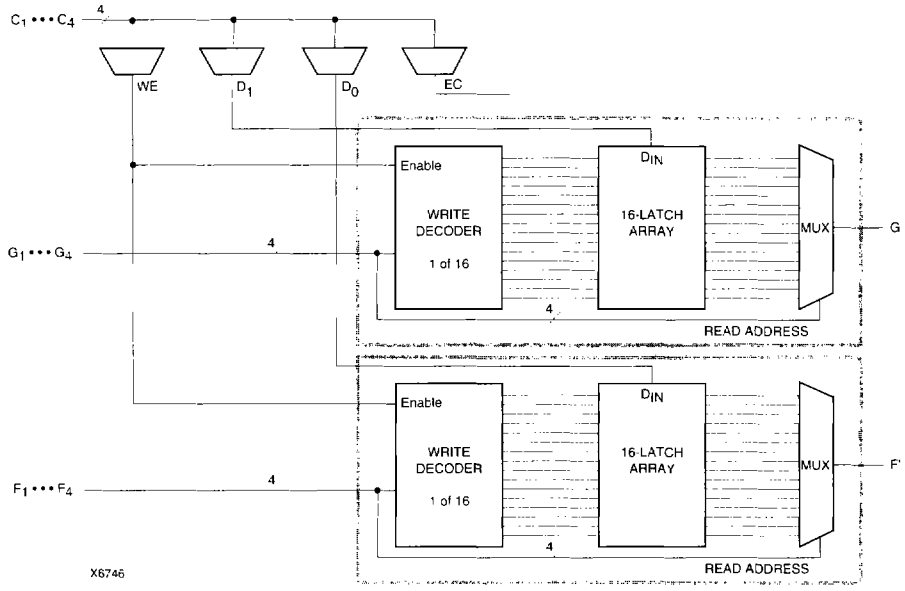


Figure 9: 16x2 (or 16x1) Level-Sensitive Single-Port RAM

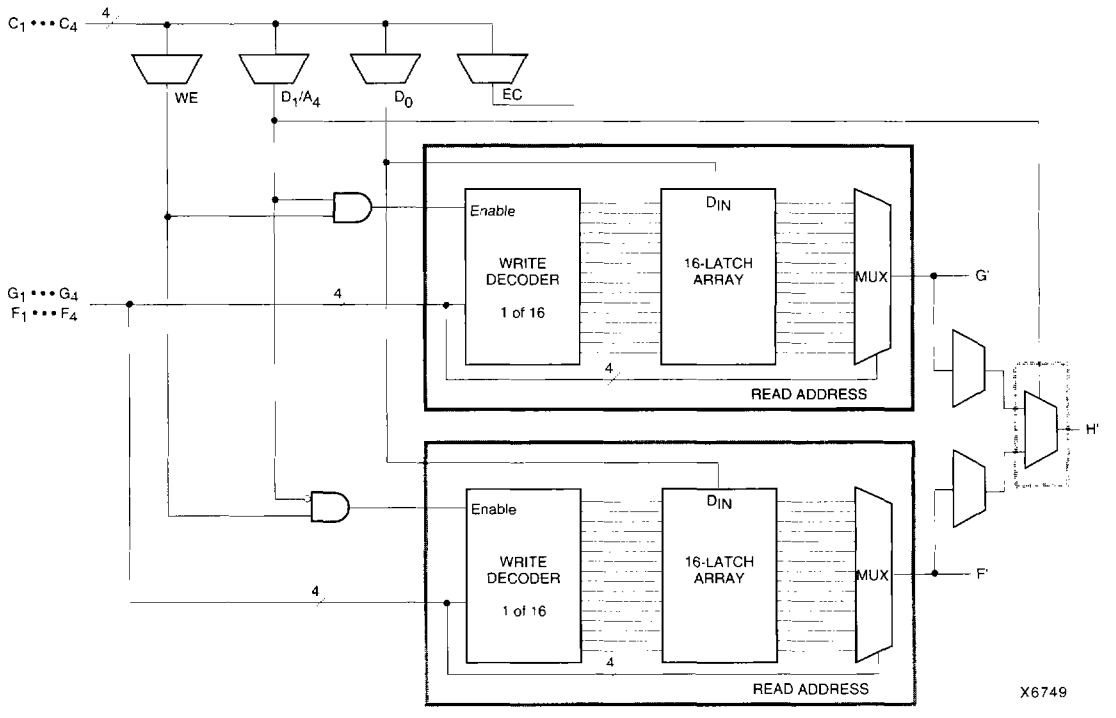


Figure 10: 32x1 Level-Sensitive Single-Port RAM (F and G addresses are identical)

Fast Carry Logic

Each CLB F and G function generator contains dedicated arithmetic logic for the fast generation of carry and borrow signals. This extra output is passed on to the function generator in the adjacent CLB. The carry chain is independent of normal routing resources.

Dedicated fast carry logic greatly increases the efficiency and performance of adders, subtractors, accumulators, comparators and counters. It also opens the door to many new applications involving arithmetic operation, where the previous generations of FPGAs were not fast enough or too inefficient. High-speed address offset calculations in microprocessor or graphics systems, and high-speed addition in digital signal processing are two typical applications.

The two 4-input function generators can be configured as a 2-bit adder with built-in hidden carry that can be expanded to any length. This dedicated carry circuitry is so fast and efficient that conventional speed-up methods like carry generate/propagate are meaningless even at the 16-bit level, and of marginal benefit at the 32-bit level.

This fast carry logic is one of the more significant features of the XC4000 Series, speeding up arithmetic and counting into the 70 MHz range.

The carry chain in XC4000E devices can run either up or down. At the top and bottom of the columns where there are no CLBs above and below, the carry is propagated to the right. (See Figure 11.) In order to improve speed in the high-capacity XC4000EX devices, which can potentially have very long carry chains, the carry chain travels upward only, as shown in Figure 12. This restriction should have little impact, because the smallest XC4000EX device, the XC4028EX, can accommodate a 64-bit carry chain in a single column. Additionally, standard interconnect can be used to route a carry signal in the downward direction.

Figure 13 on page 22 shows an XC4000E CLB with dedicated fast carry logic. The carry logic in the XC4000EX is similar, except that COUT exits at the top only, and the signal CINDOWN does not exist. As shown in Figure 13, the carry logic shares operand and control inputs with the function generators. The carry outputs connect to the function generators, where they are combined with the operands to form the sums.

Figure 14 and Figure 15 on page 23 show the details of the carry logic for the XC4000E and the XC4000EX respectively. These diagrams show the contents of the box labeled "CARRY LOGIC" in Figure 13. As shown, the XC4000EX carry logic eliminated a multiplexer to reduce delay on the pass-through carry chain. Additionally, the multiplexer on the G4 path now has a memory-programmable input, which permits G4 to directly connect to COUT. G4 thus becomes an additional high-speed initialization path for carry-in.

The dedicated carry logic is discussed in detail in Xilinx document XAPP 013: "*Using the Dedicated Carry Logic in XC4000.*" This discussion also applies to XC4000E devices, and to XC4000EX devices when the minor logic changes are taken into account.

The fast carry logic can be accessed by placing special library symbols, or by using Xilinx Relationally Placed Macros (RPMs) that already include these symbols.

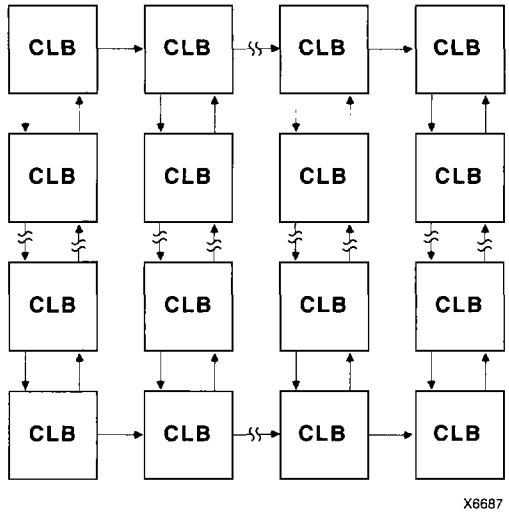


Figure 11: Available XC4000E Carry Propagation Paths

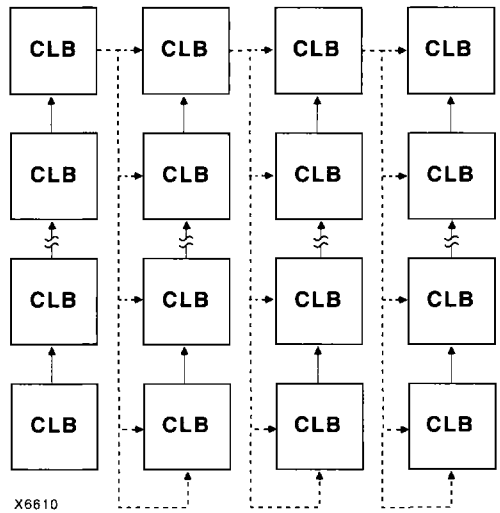


Figure 12: Available XC4000EX Carry Propagation Paths (dotted lines use general interconnect)

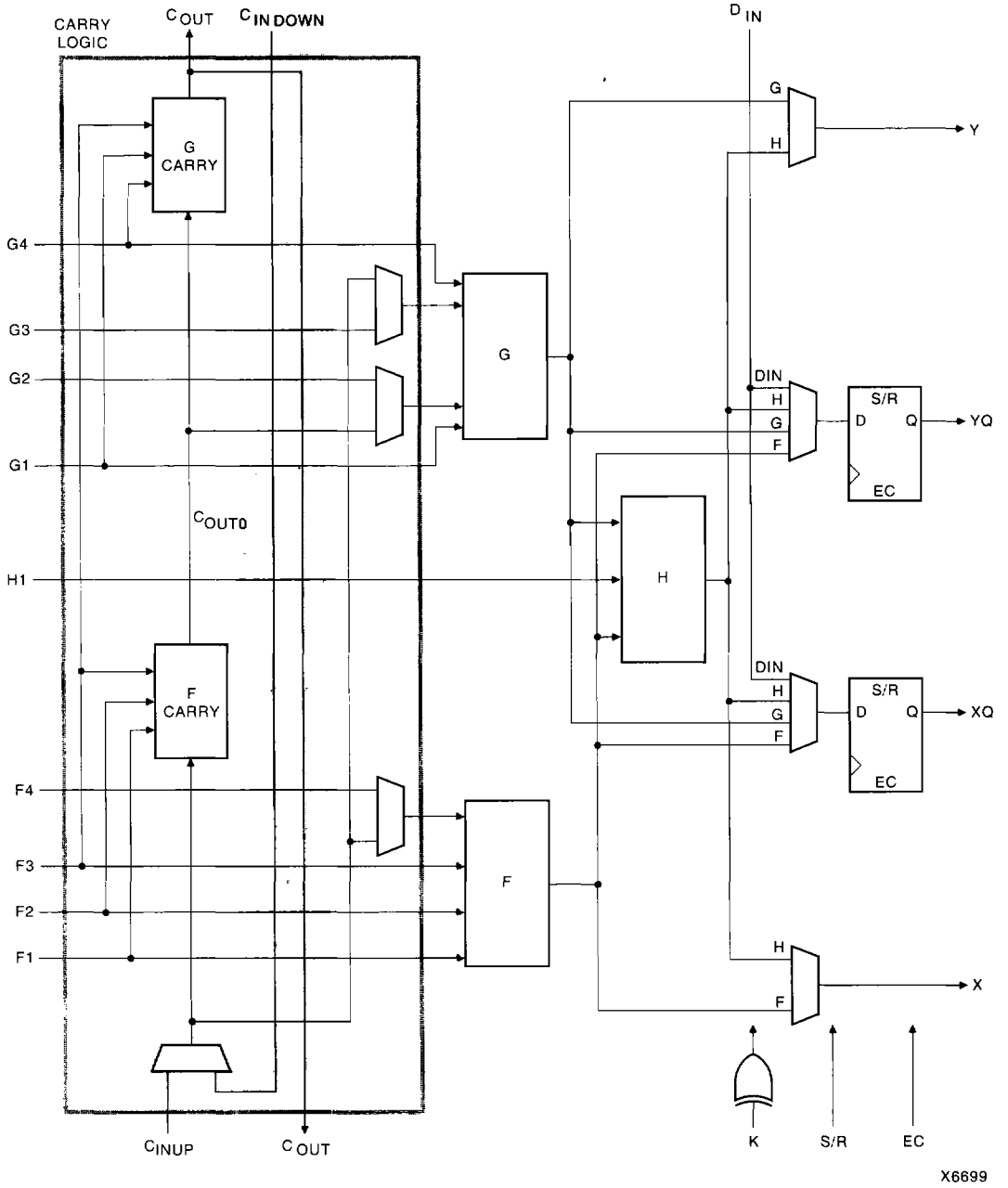


Figure 13: Fast Carry Logic in XC4000E CLB (shaded area not present in XC4000EX)

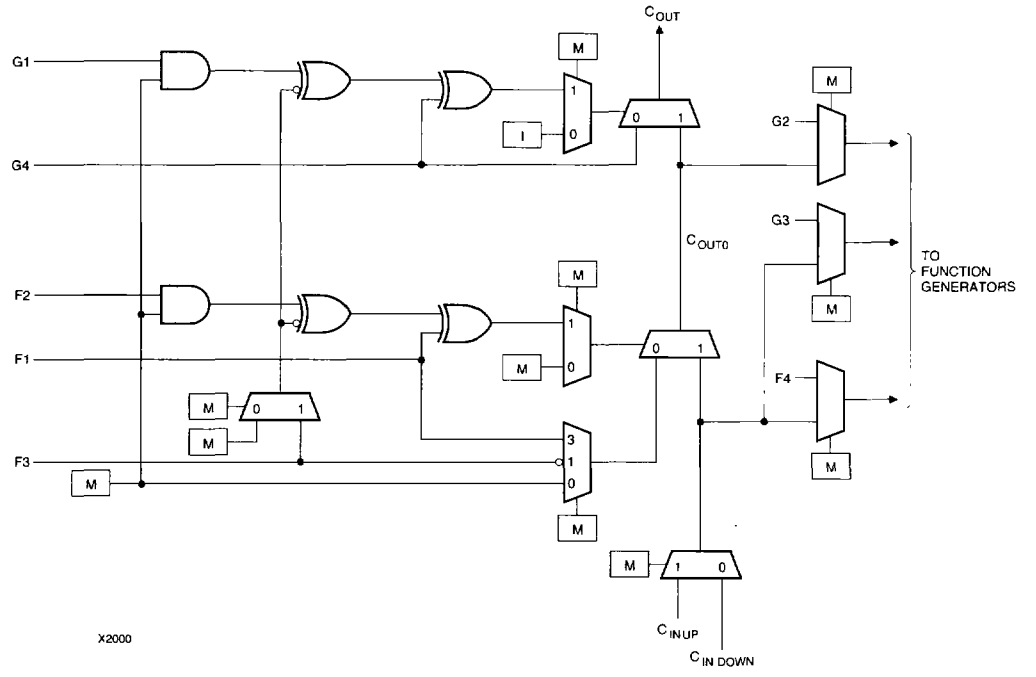


Figure 14: Detail of XC4000E Dedicated Carry Logic

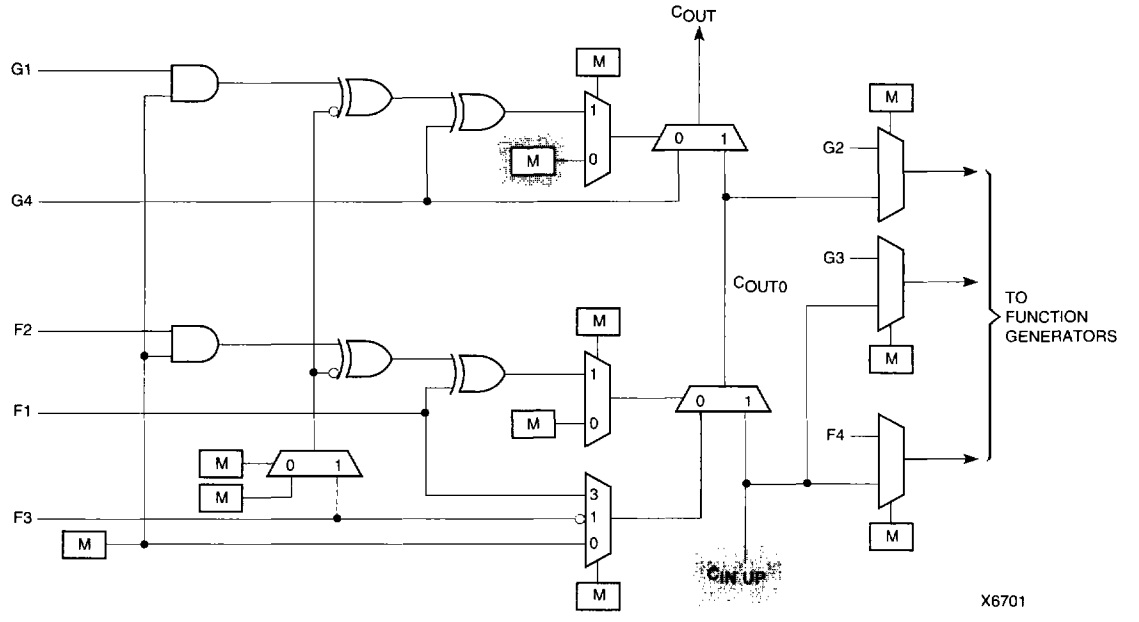


Figure 15: Detail of XC4000EX Dedicated Carry Logic (shaded areas show differences from XC4000E carry logic)

Input/Output Blocks (IOBs)

User-configurable input/output blocks (IOBs) provide the interface between external package pins and the internal logic. Each IOB controls one package pin and can be configured for input, output, or bidirectional signals.

Figure 16 shows a simplified block diagram of the XC4000E IOB. A more complete diagram of the XC4000E IOB can be found in Figure 42 on page 51, in the "Boundary Scan" section. Figure 42 includes the boundary scan logic in the IOB.

Figure 17 shows a simplified block diagram of the XC4000EX IOB. The XC4000EX IOB contains some special features not included in the XC4000E IOB. These features are highlighted in Figure 17, and discussed throughout this section. When XC4000EX special features are discussed, they are clearly identified in the text. Any feature not so identified is present in both XC4000E and XC4000EX devices.

IOB Input Signals

Two paths, labeled I1 and I2 in Figure 16 and Figure 17, bring input signals into the array. Inputs also connect to an input register that can be programmed as either an edge-triggered flip-flop or a level-sensitive latch.

The choice is made by placing the appropriate library symbol. For example, IFD is the basic input flip-flop (rising edge triggered), and ILD is the basic input latch (transparent-High). Variations with inverted clocks are available, and some combinations of latches and flip-flops can be implemented in a single IOB, as described in the *XACT Libraries Guide*.

The inputs can be globally configured for either TTL (1.2V, default) or CMOS thresholds, using an option in the Make-Bits program. There is a slight hysteresis of about 300mV. The output levels are also configurable; the two global adjustments of input threshold and output level are independent.

Inputs of the low-voltage devices *must* be configured as CMOS at all times. They can be driven by the outputs of all 5-Volt XC4000-Series devices, provided that the 5-Volt outputs are in TTL mode. They can also be driven by any TTL output that does not exceed 3.7 V. 5-Volt XC3000-family device outputs, for example, are TTL-compatible, but since the output voltage can exceed 3.7 V, they cannot be used to drive an XC4000L or XC4000XL input.

The inputs of XC4000-Series 5-Volt devices can be driven by the outputs of any 3.3-Volt device, if the 5-Volt inputs are in TTL mode.

Supported sources for XC4000-Series device inputs are shown in Table 10.

Table 10: Supported Sources for XC4000-Series Device Inputs

Source	XC4000-Series Inputs		
	3.3 V, CMOS	5 V, TTL	5 V, CMOS
Any device, Vcc = 3.3 V, CMOS outputs	√	√	**Unreliable Data**
XC4000-Series, Vcc = 5 V, TTL outputs	√	√	
Any device, Vcc = 5 V, TTL outputs (Voh ≤ 3.7 V)	√	√	
Any device, Vcc = 5 V, CMOS outputs	**Danger**[1]	√	√

1. Acceptable for XC4000XL if the designated 5-Volt supply pad (V_{TT}) is tied to 5V.

Registered Inputs

The I1 and I2 signals that exit the block can each carry either the direct or registered input signal.

The input and output storage elements in each IOB have a common clock enable input, which, through configuration, can be activated individually for the input or output flip-flop, or both. This clock enable operates exactly like the EC pin on the XC4000-Series CLB. It cannot be inverted within the IOB.

The storage element behavior is shown in Table 11.

Table 11: Input Register Functionality (active rising edge is shown)

Mode	Clock	Clock Enable	D	Q
Power-Up or GSR	X	X	X	SR
Flip-Flop	_/‾	1*	D	D
	0	X	X	Q
Latch	1	1*	X	Q
	0	1*	D	D
Both	X	0	X	Q

Legend:

X	Don't care
_/‾	Rising edge
SR	Set or Reset value. Reset is default.
0*	Input is Low or unconnected (default value)
1*	Input is High or unconnected (default value)

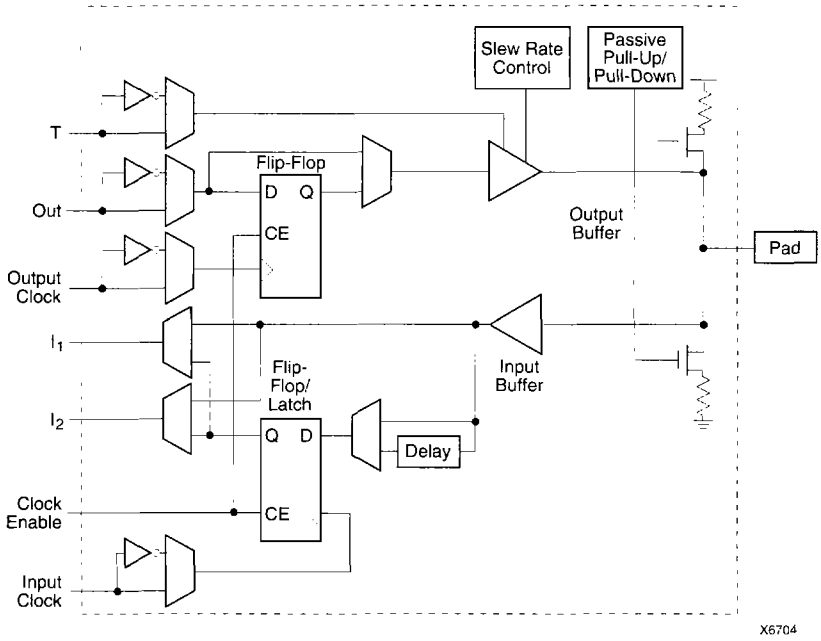


Figure 16: Simplified Block Diagram of XC4000E IOB

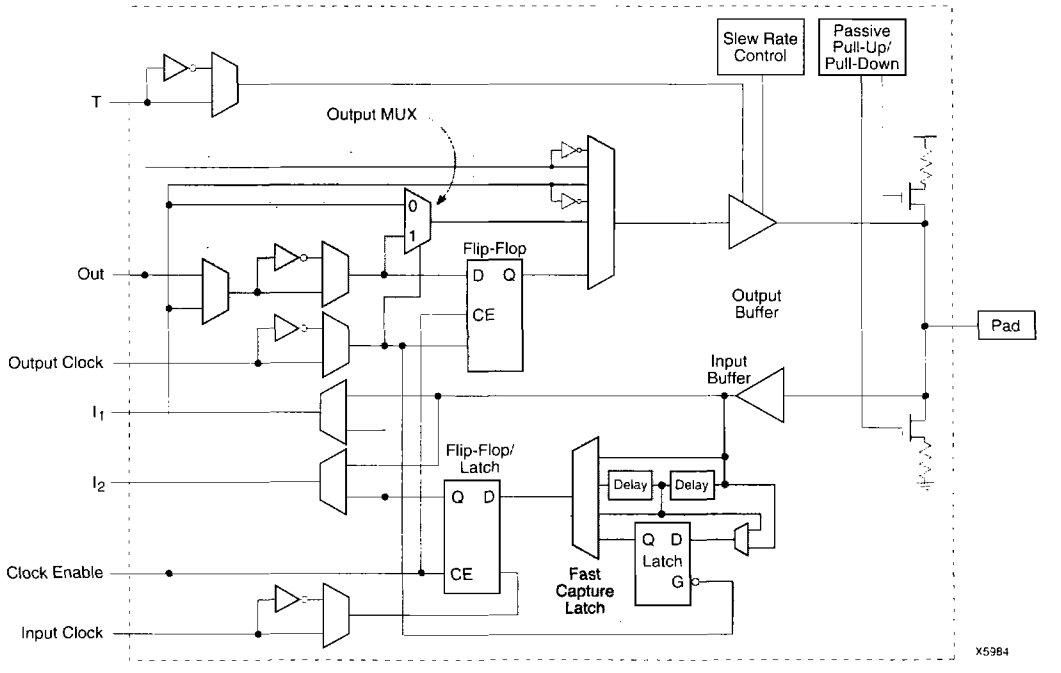


Figure 17: Simplified Block Diagram of XC4000EX IOB (shaded areas indicate differences from XC4000E)

Optional Delay Guarantees Zero Hold Time

The data input to the register can optionally be delayed by several nanoseconds. With the delay enabled, the setup time of the input flip-flop is increased so that normal clock routing does not result in a positive hold-time requirement. A positive hold time requirement can lead to unreliable, temperature- or processing-dependent operation.

The input flip-flop setup time is defined between the data measured at the device I/O pin and the clock input at the IOB (not at the clock pin). Any routing delay from the device clock pin to the clock input of the IOB must, therefore, be subtracted from this setup time to arrive at the real setup time requirement relative to the device pins. A short specified setup time might, therefore, result in a negative setup time at the device pins, i.e., a positive hold-time requirement.

When a delay is inserted on the data line, more clock delay can be tolerated without causing a positive hold-time requirement. Sufficient delay eliminates the possibility of a data hold-time requirement at the external pin. The maximum delay is therefore inserted as the default.

The XC4000E IOB has a one-tap delay element: either the delay is inserted (default), or it is not. The delay guarantees a zero hold time with respect to clocks routed through any of the XC4000E global clock buffers. (See "Global Nets and Buffers (XC4000E only)" on page 41 for a description of the global clock buffers in the XC4000E.) For a shorter input register setup time, with non-zero hold, attach a NODELAY attribute or property to the flip-flop.

The XC4000EX IOB has a two-tap delay element, with choices of a full delay, a partial delay, or no delay. The attributes or properties used to select the desired delay are shown in Table 12. The choices are no added attribute, MEDDELAY, and NODELAY. The default setting, with no added attribute, ensures no hold time with respect to any of the XC4000EX clock buffers, including the Global Low-Skew buffers. MEDDELAY ensures no hold time with respect to the Global Early and FastCLK buffers. Inputs with NODELAY may have a positive hold time with respect to all clock buffers, including the FastCLK buffers. For a description of each of these buffers, see "Global Nets and Buffers (XC4000EX only)" on page 43.

Table 12: XC4000EX IOB Input Delay Element

Value	When to Use
full delay (default, no attribute added)	Zero Hold with respect to Global Low-Skew Buffer, Global Early Buffer, or FastCLK Buffer
MEDDELAY	Zero Hold with respect to Global Early Buffer or FastCLK Buffer
NODELAY	Short Setup, positive Hold time

Additional Input Latch for Fast Capture (XC4000EX only)

The XC4000EX IOB has an additional optional latch on the input. This latch, as shown in Figure 17, is clocked by the output clock — the clock used for the output flip-flop — rather than the input clock. Therefore, two different clocks can be used to clock the two input storage elements. This additional latch allows the very fast capture of input data, which is then synchronized to the internal clock by the IOB flip-flop or latch.

To use this Fast Capture technique, drive the output clock pin (the Fast Capture latching signal) from the output of one of the Global Early or FastCLK buffers supplied in the XC4000EX. The second storage element should be clocked by a Global Low-Skew buffer, to synchronize the incoming data to the internal logic. (See Figure 18.) These special buffers are described in "Global Nets and Buffers (XC4000EX only)" on page 43.

The Fast Capture latch is designed primarily for use with a Global Early buffer. For Fast Capture, a single clock signal is routed through both a Global Early buffer and a Global Low-Skew buffer. (The two buffers share an input pad.) The Fast Capture latch is clocked by the Global Early buffer, and the standard IOB flip-flop or latch is clocked by the Global Low-Skew buffer. This mode is the safest way to use the Fast Capture latch, because the clock buffers on both storage elements are driven by the same pad. There is no external skew between clock pads to create potential problems.

Alternatively, a FastCLK buffer can be used to minimize the setup time of device inputs, if a positive hold time is acceptable. Use the FastCLK buffer to clock the Fast Capture latch, and a slower clock buffer to clock the standard IOB flip-flop or latch. Either the Global Early buffer or the Global Low-Skew buffer can be used for the second storage ele-

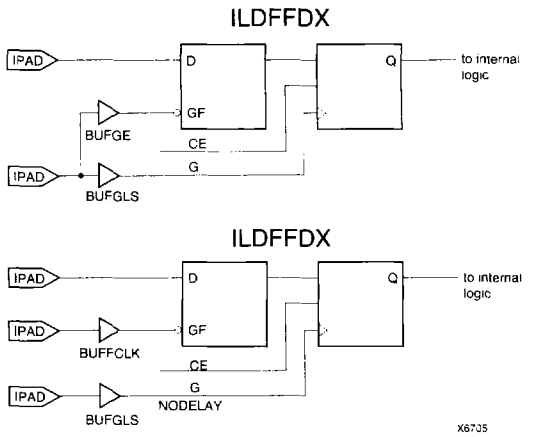


Figure 18: Examples Using XC4000EX Fast Capture Latch

ment, but whichever one is used should be the same clock as the related internal logic. Since the FastCLK pads are different from the Global Early and Global Low-Skew pads, care must be taken to ensure that skew external to the device does not create internal timing difficulties.

To place the Fast Capture latch in a design, use one of the special library symbols, ILDFFDX or ILDFLDX. ILDFFDX is a transparent-Low Fast Capture latch followed by an active-High input flip-flop. ILDFLDX is a transparent-Low Fast Capture latch followed by a transparent-High input latch. Any of the clock inputs can be inverted before driving the library element, and the inverter is absorbed into the IOB. If a single BUFG output is used to drive both clock inputs, the software automatically runs the clock through both a Global Low-Skew buffer and a Global Early buffer, and clocks the Fast Capture latch appropriately.

Figure 17 on page 25 also shows a two-tap delay on the input. By default, if the Fast Capture latch is used, the Xilinx software assumes a Global Early buffer is driving the clock, and selects MEDDELAY to ensure a zero hold time. This default can be overridden to remove the delay, if FastClk is used, by attaching a NODELAY attribute or property to the ILDFFD or ILDFLD latch. Select the desired delay based on the discussion in the previous subsection.

IOB Output Signals

Output signals can be optionally inverted within the IOB, and can pass directly to the pad or be stored in an edge-triggered flip-flop. The functionality of this flip-flop is shown in Table 13.

An active-High 3-state signal can be used to place the output buffer in a high-impedance state, implementing 3-state outputs or bidirectional I/O. Under configuration control, the output (OUT) and output 3-state (T) signals can be inverted. The polarity of these signals is independently configured for each IOB.

The 4-mA maximum output current specification of many FPGAs often forces the user to add external buffers, which are especially cumbersome on bidirectional I/O lines. The XC4000E and XC4000EX devices solve many of these problems by providing a guaranteed output sink current of 12 mA. Two adjacent outputs can be interconnected externally to sink up to 24 mA. (XC4000L and XC4000XL outputs can sink up to 4 mA, and two adjacent XC4000L and XC4000XL outputs can sink up to 8 mA.) The XC4000E and XC4000EX FPGAs can thus directly drive buses on a printed circuit board.

Table 13: Output Flip-Flop Functionality (active rising edge is shown)

Mode	Clock	Clock Enable	T	D	Q
Power-Up or GSR	X	X	0*	X	SR
Flip-Flop	X	0	0*	X	Q
	⎍/⎍	1*	0*	D	D
	X	X	1	X	Z
	0	X	0*	X	Q

Legend:

X	Don't care
⎍/⎍	Rising edge
SR	Set or Reset value. Reset is default.
0*	Input is Low or unconnected (default value)
1*	Input is High or unconnected (default value)
Z	3-state

By default, the output pull-up structure is configured as a TTL-like totem-pole. The High driver is an n-channel pull-up transistor, pulling to a voltage one transistor threshold below Vcc. Alternatively, the outputs can be globally configured as CMOS drivers, with p-channel pull-up transistors pulling to Vcc. This MakeBits option applies to all outputs on the device. It is not individually programmable.

Outputs of low-voltage devices *must* be configured as CMOS at all times. They can drive the inputs of any 5-Volt device with TTL-compatible thresholds.

Any XC4000-Series 5-Volt device with its outputs configured in TTL mode can drive the inputs of any typical 3.3-Volt device.

Supported destinations for XC4000-Series device outputs are shown in Table 14.

Table 14: Supported Destinations for XC4000-Series Outputs

Destination	XC4000-Series Outputs		
	3.3 V, CMOS	5 V, TTL	5 V, CMOS
Any typical device, Vcc = 3.3 V, CMOS-threshold inputs	√	√	some[1]
Any device, Vcc = 5 V, TTL-threshold inputs	√	√	√
Any device, Vcc = 5 V, CMOS-threshold inputs	**Unreliable Data**		√

1. Only if destination device has 5-V tolerant inputs

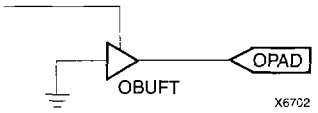


Figure 19: Open-Drain Output

An output can be configured as open-drain (open-collector) by placing an OBUFT symbol in a schematic or HDL code, then tying the 3-state pin (T) to the output signal, and the input pin (I) to Ground. (See Figure 19.)

Output Slew Rate

The slew rate of each output buffer is, by default, reduced, to minimize power bus transients when switching non-critical signals. For critical signals, attach a FAST attribute or property to the output buffer or flip-flop.

For XC4000E devices, maximum total capacitive load for simultaneous fast mode switching in the same direction is 200 pF for all package pins between each Power/Ground pin pair. For XC4000EX devices, additional internal Power/Ground pin pairs are connected to special Power and Ground planes within the packages, to reduce ground bounce. Therefore, the maximum total capacitive load is 300 pF between each external Power/Ground pin pair. Maximum loading may vary for the low-voltage devices.

For slew-rate limited outputs this total is two times larger for each device type: 400 pF for XC4000E devices and 600 pF for XC4000EX devices. This maximum capacitive load should not be exceeded, as it can result in ground bounce of greater than 1.5 V amplitude and more than 5 ns duration. This level of ground bounce may cause undesired transient behavior on an output, or in the internal logic. This restriction is common to all high-speed digital ICs, and is not particular to Xilinx or the XC4000 Series.

XC4000-Series devices have a feature called "Soft Startup," designed to reduce ground bounce when all outputs are turned on simultaneously at the end of configuration. When the configuration process is finished and the device starts up, the first activation of the outputs is automatically slew-rate limited. Immediately following the initial activation of the I/O, the slew rate of the individual outputs is determined by the individual configuration option for each IOB.

Global Three-State

A separate Global 3-State line (not shown in Figure 16 or Figure 17) forces all FPGA outputs to the high-impedance state, unless boundary scan is enabled and is executing an EXTEST instruction. This global net (GTS) does not compete with other routing resources; it uses a dedicated distribution network.

GTS can be driven from any user-programmable pin as a global 3-state input. To use this global net, place an input pad and input buffer in the schematic or HDL code, driving the GTS pin of the STARTUP symbol. A specific pin location can be assigned to this input using a LOC attribute or property, just as with any other user-programmable pad. An inverter can optionally be inserted after the input buffer to invert the sense of the Global 3-State signal. Using GTS is similar to GSR. See Figure 2 on page 13 for details.

Alternatively, GTS can be driven from any internal node.

Output Multiplexer/2-Input Function Generator (XC4000EX only)

As shown in Figure 17 on page 25, the output path in the XC4000EX IOB contains an additional multiplexer not available in the XC4000E IOB. The multiplexer can also be configured as a 2-input function generator, implementing a pass-gate, AND-gate, OR-gate, or XOR-gate, with 0, 1, or 2 inverted inputs. The logic used to implement these functions is shown in the upper gray area of Figure 17.

When configured as a multiplexer, this feature allows two output signals to time-share the same output pad; effectively doubling the number of device outputs without requiring a larger, more expensive package.

When the MUX is configured as a 2-input function generator, logic can be implemented within the IOB itself. Combined with either a FastCLK or Global Early buffer, this arrangement allows very high-speed gating of a single signal. For example, a wide decoder can be implemented in CLBs, and its output gated with a Read or Write Strobe driven by a FastCLK buffer, as shown in Figure 20. The critical-path pin-to-pin delay of this circuit is less than 6 nanoseconds. (This value may not be achievable in XC4000XL devices.)

As shown in Figure 17, the IOB input pins Out, Output Clock, and Clock Enable have different delays and different flexibilities regarding polarity. Additionally, Output Clock sources are more limited than the other inputs. Therefore, the Xilinx software does not move logic into the IOB function generators unless explicitly directed to do so.

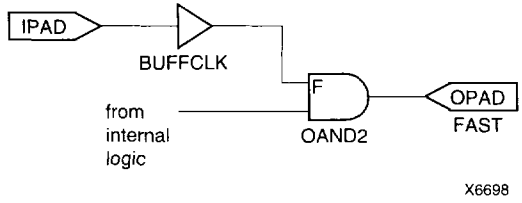


Figure 20: Fast Pin-to-Pin Path in XC4000E

Figure 21: Output AND and MUX Symbols in XC4000EX IOB

The user can specify that the IOB function generator be used, by placing special library symbols beginning with the letter "O." For example, a 2-input AND-gate in the IOB function generator is called OAND2. Use the symbol input pin labelled "F" for the signal on the critical path. This signal is placed on the OK pin — the IOB input with the shortest delay to the function generator. Two examples are shown in Figure 21.

Other IOB Options

There are a number of other programmable options in the XC4000-Series IOB.

Pull-up and Pull-down Resistors

Programmable pull-up and pull-down resistors are useful for tying unused pins to Vcc or Ground to minimize power consumption and reduce noise sensitivity. The configurable pull-up resistor is a p-channel transistor that pulls to Vcc. The configurable pull-down resistor is an n-channel transistor that pulls to Ground.

The value of these resistors is 50 kΩ – 100 kΩ. This high value makes them unsuitable as wired-AND pull-up resistors.

The pull-up resistors for most user-programmable IOBs are active during the configuration process. See Table 24 on page 78 for a list of pins with pull-ups active before and during configuration.

After configuration, voltage levels of unused pads, bonded or unbonded, must be valid logic levels, to reduce noise sensitivity and avoid excess current. Therefore, by default, unused pads are configured with the internal pull-up resistor active. Alternatively, they can be individually configured with the pull-down resistor, or as a driven output, or to be driven by an external source. To activate the internal pull-up, attach the PULLUP library component to the net attached to the pad. To activate the internal pull-down, attach the PULLDOWN library component to the net attached to the pad.

Independent Clocks

Separate clock signals are provided for the input and output flip-flops. The clock can be independently inverted for each flip-flop within the IOB, generating either falling-edge or rising-edge triggered flip-flops. The clock inputs for each IOB are independent, except that in the XC4000EX, the Fast Capture latch shares an IOB input with the output clock pin.

Early Clock for IOBs (XC4000EX only)

Special early clocks are available for IOBs. These clocks are sourced by the same sources as the Global Low-Skew buffers, but are separately buffered. They have fewer loads and therefore less delay. The early clock can drive either the IOB output clock or the IOB input clock, or both. The early clock allows fast capture of input data, and fast clock-to-output on output data. The Global Early buffers that drive these clocks are described in "Global Nets and Buffers (XC4000EX only)" on page 43.

Fast Clock for IOBs (XC4000EX only)

Very fast clocks driven by FastCLK buffers are also available for IOBs. These clocks are sourced by semi-dedicated pads—the pads can be used as general I/O if not used to drive FastCLK buffers. There are two FastCLK buffers on the left edge, and two on the right edge of the device. They provide the fastest method of reaching the IOB clock pins. The FastCLK buffer can drive either the IOB output clock or the IOB input clock, or both. These buffers allow the fastest possible setup times and clock-to-output times. The FastCLK buffers are described in "Global Nets and Buffers (XC4000EX only)" on page 43.

Global Set/Reset

As with the CLB registers, the Global Set/Reset signal (GSR) can be used to set or clear the input and output registers, depending on the value of the INIT attribute or property. The two flip-flops can be individually configured to set or clear on reset and after configuration. Other than the global GSR net, no user-controlled set/reset signal is available to the I/O flip-flops. The choice of set or clear applies to both the initial state of the flip-flop and the response to the Global Set/Reset pulse. See "Global Set/Reset" on page 13 for a description of how to use GSR.

JTAG Support

Embedded logic attached to the IOBs contains test structures compatible with IEEE Standard 1149.1 for boundary scan testing, permitting easy chip and board-level testing. More information is provided in "Boundary Scan" on page 50.

Three-State Buffers

A pair of 3-state buffers is associated with each CLB in the array. (See Figure 27 on page 34.) These 3-state buffers can be used to drive signals onto the nearest horizontal longlines above and below the CLB. They can therefore be used to implement multiplexed or bidirectional buses on the horizontal longlines, saving logic resources. Programmable pull-up resistors attached to these longlines help to implement a wide wired-AND function.

The buffer enable is an active-High 3-state (i.e. an active-Low enable), as shown in Table 15.

Another 3-state buffer with similar access is located near each I/O block along the right and left edges of the array. (See Figure 33 on page 39.)

The horizontal longlines driven by the 3-state buffers have a weak keeper at each end. This circuit prevents undefined floating levels. However, it is overridden by any driver, even a pull-up resistor.

Special longlines running along the perimeter of the array can be used to wire-AND signals coming from nearby IOBs or from internal longlines. These longlines form the wide edge decoders discussed in "Wide Edge Decoders" on page 31.

Three-State Buffer Modes

The 3-state buffers can be configured in three modes:

- Standard 3-state buffer
- Wired-AND with input on the I pin
- Wired OR-AND

Standard 3-State Buffer

All three pins are used. Place the library element BUFT. Connect the input to the I pin and the output to the O pin. The T pin is an active-High 3-state (i.e. an active-Low enable). Tie the T pin to Ground to implement a standard buffer.

Wired-AND with Input on the I Pin

The buffer can be used as a Wired-AND. Use the WAND1 library symbol, which is essentially an open-drain buffer. WAND4, WAND8, and WAND16 are also available. See the *XACT Libraries Guide* for further information.

The T pin is internally tied to the I pin. Connect the input to the I pin and the output to the O pin. Connect the outputs of all the WAND1s together and attach a PULLUP symbol.

Wired OR-AND

The buffer can be configured as a Wired OR-AND. A High level on either input turns off the output. Use the WOR2AND library symbol, which is essentially an open-drain 2-input OR gate. The two input pins are functionally equivalent. Attach the two inputs to the I0 and I1 pins and tie the output to the O pin. Tie the outputs of all the WOR2ANDs together and attach a PULLUP symbol.

Three-State Buffer Examples

Figure 22 shows how to use the 3-state buffers to implement a wired-AND function. When all the buffer inputs are High, the pull-up resistor(s) provide the High output.

Figure 23 shows how to use the 3-state buffers to implement a multiplexer. The selection is accomplished by the buffer 3-state signal.

Pay particular attention to the polarity of the T pin when using these buffers in a design. Active-High 3-state (T) is identical to an active-Low output enable, as shown in Table 15.

Table 15: Three-State Buffer Functionality

IN	T	OUT
X	1	Z
IN	0	IN

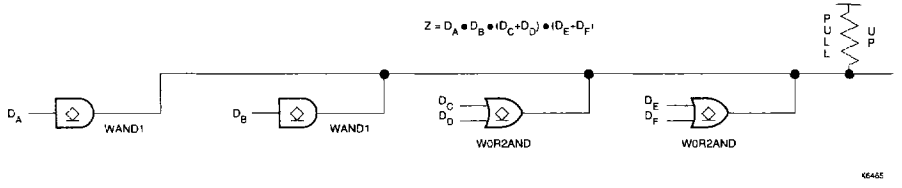


Figure 22: Open-Drain Buffers Implement a Wired-AND Function

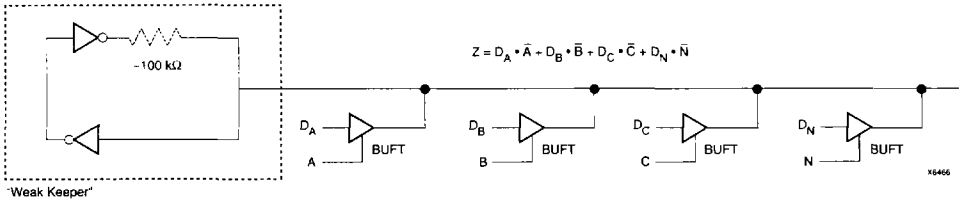


Figure 23: 3-State Buffers Implement a Multiplexer

Wide Edge Decoders

Dedicated decoder circuitry boosts the performance of wide decoding functions. When the address or data field is wider than the function generator inputs, FPGAs need multi-level decoding and are thus slower than PALs. XC4000-Series CLBs have nine inputs. Any decoder of up to nine inputs is, therefore, compact and fast. However, there is also a need for much wider decoders, especially for address decoding in large microprocessor systems.

An XC4000-Series FPGA has four programmable decoders located on each edge of the device. The inputs to each decoder are any of the IOB I1 signals on that edge plus one local interconnect per CLB row or column. Each row or column of CLBs provides up to three variables or their compliments., as shown in Figure 24. Each decoder generates a High output (resistor pull-up) when the AND condition of the selected inputs, or their complements, is true. This is analogous to a product term in typical PAL devices.

Each of these wired-AND gates is capable of accepting up to 42 inputs on the XC4005E and 72 on the XC4013E. There are up to 96 inputs for each decoder on the XC4028EX and 132 on the XC4052EX. The decoders may also be split in two when a larger number of narrower decoders are required, for a maximum of 32 decoders per device.

The decoder outputs can drive CLB inputs, so they can be combined with other logic to form a PAL-like AND/OR structure. The decoder outputs can also be routed directly to the chip outputs. For fastest speed, the output should be on the same chip edge as the decoder. Very large PALs can be emulated by ORing the decoder outputs in a CLB. This decoding feature covers what has long been considered a weakness of older FPGAs. Users often resorted to external PALs for simple but fast decoding functions. Now, the dedicated decoders in the XC4000-Series device can implement these functions fast and efficiently.

To use the wide edge decoders, place one or more of the WAND library symbols (WAND1, WAND4, WAND8, WAND16). Attach a DECODE attribute or property to each WAND symbol. Tie the outputs together and attach a PULLUP symbol. Location attributes or properties such as L (left edge) or TR (right half of top edge) should also be used to ensure the correct placement of the decoder inputs.

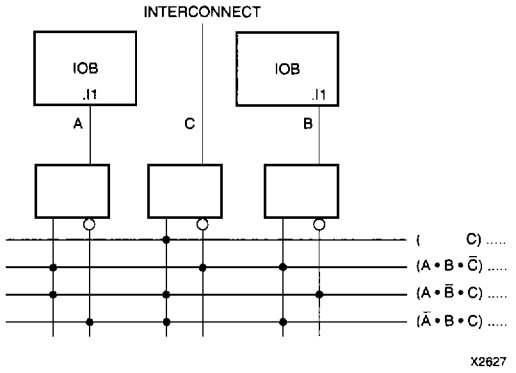


Figure 24: XC4000-Series Edge Decoding Example

On-Chip Oscillator

XC4000-Series devices include an internal oscillator. This oscillator is used to clock the power-on time-out, for configuration memory clearing, and as the source of CCLK in Master configuration modes. The oscillator runs at a nominal 8 MHz frequency that varies with process, Vcc, and temperature. The output frequency falls between 4 and 10 MHz. (The oscillator operates more slowly at lower voltages. The output frequency may be reduced by as much as 10% for low-voltage devices.)

The oscillator output is optionally available after configuration. Any two of four resynchronized taps of a built-in divider are also available. These taps are at the fourth, ninth, fourteenth and nineteenth bits of the divider. Therefore, if the primary oscillator output is running at the nominal 8 MHz, the user has access to an 8 MHz clock, plus any two of 500 kHz, 16kHz, 490Hz and 15Hz (up to 10% lower for low-voltage devices). These frequencies can vary by as much as -50% or +25%.

These signals can be accessed by placing the OSC4 library element in a schematic or in HDL code (see Figure 25).

The oscillator is automatically disabled after configuration if the OSC4 symbol is not used in the design.

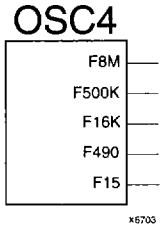


Figure 25: XC4000-Series Oscillator Symbol

Programmable Interconnect

All internal connections are composed of metal segments with programmable switching points and switching matrices to implement the desired routing. A structured, hierarchical matrix of routing resources is provided to achieve efficient automated routing.

The XC4000E and XC4000EX share a basic interconnect structure. XC4000EX devices, however, have additional routing not available in the XC4000E. The extra routing resources allow high utilization in high-capacity devices. All XC4000EX-specific routing resources are clearly identified throughout this section. Any resources not identified as XC4000EX-specific are present in all XC4000-Series devices.

This section describes the varied routing resources available in XC4000-Series devices. The implementation software automatically assigns the appropriate resources based on the density and timing requirements of the design.

Interconnect Overview

There are several types of interconnect.

- CLB routing is associated with each row and column of the CLB array.
- IOB routing forms a ring (called a VersaRing) around the outside of the CLB array. It connects the I/O with the internal logic blocks.
- Global routing consists of dedicated networks primarily designed to distribute clocks throughout the device with minimum delay and skew. Global routing can also be used for other high-fanout signals.

Five interconnect types are distinguished by the relative length of their segments: single-length lines, double-length lines, quad and octal lines (XC4000EX only), and longlines. In the XC4000EX, direct connects allow fast data flow between adjacent CLBs, and between IOBs and CLBs.

Extra routing is included in the IOB pad ring. The XC4000EX also includes a ring of octal interconnect lines near the IOBs to improve pin-swapping and routing to locked pins.

XC4000E devices include two types of global buffers, while XC4000EX devices have three different types. These global buffers have different properties, and are intended for different purposes. They are discussed in detail later in this section.

CLB Routing Connections

A high-level diagram of the routing resources associated with one CLB is shown in Figure 26. The shaded arrows represent routing present only in XC4000EX devices.

Table 16 shows how much routing of each type is available in XC4000E and XC4000EX CLB arrays. Clearly, very large designs, or designs with a great deal of interconnect, will route more easily in the XC4000EX. Smaller XC4000E designs, typically requiring significantly less interconnect, do not require the additional routing.

Figure 27 on page 34 is a detailed diagram of both the XC4000E and the XC4000EX CLB, with associated routing. The shaded square is the programmable switch matrix, present in both the XC4000E and the XC4000EX. The L-shaped shaded area is present only in XC4000EX devices. As shown in the figure, the XC4000EX block is essentially an XC4000E block with additional routing.

CLB inputs and outputs are distributed on all four sides, providing maximum routing flexibility. In general, the entire architecture is symmetrical and regular. It is well suited to established placement and routing algorithms. Inputs, outputs, and function generators can freely swap positions within a CLB to avoid routing congestion during the placement and routing operation.

Table 16: Routing per CLB in XC4000-Series Devices

	XC4000E		XC4000EX	
	Vertical	**Horizontal**	**Vertical**	**Horizontal**
Singles	8	8	8	8
Doubles	4	4	4	4
Quads	0	0	12	12
Longlines	6	6	10	6
Direct Connects	0	0	2	2
Globals	4	0	8	0
Carry Logic	2	0	1	0
Total	24	18	45	32

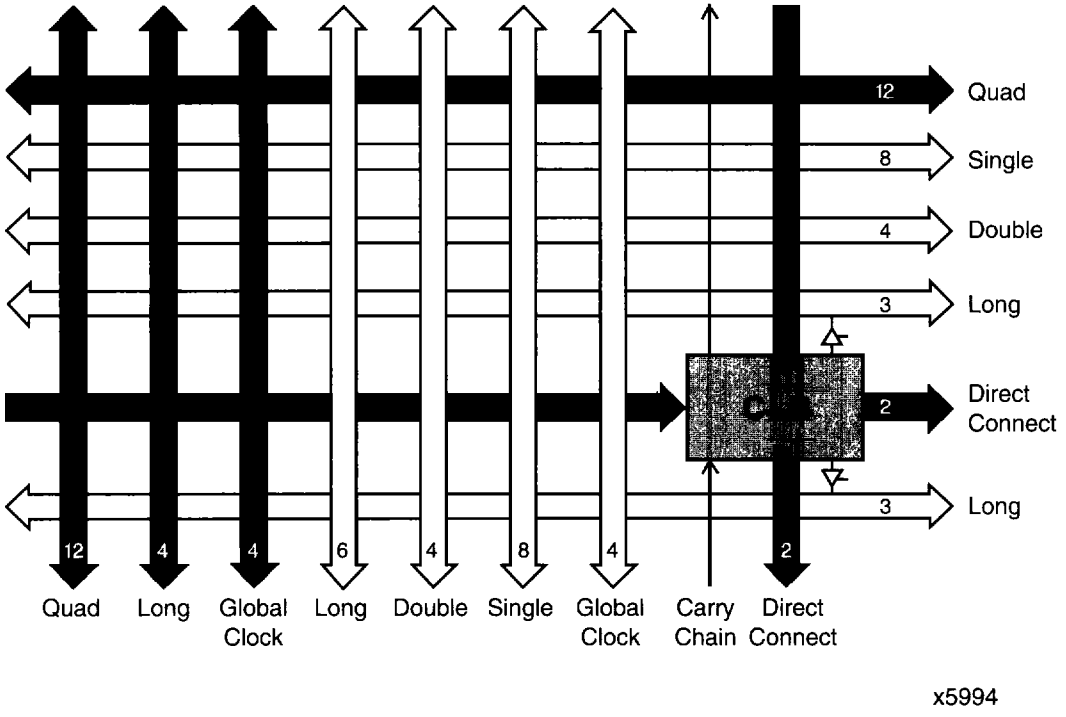


Figure 26: High-Level Routing Diagram of XC4000-Series CLB (shaded arrows indicate XC4000EX only)

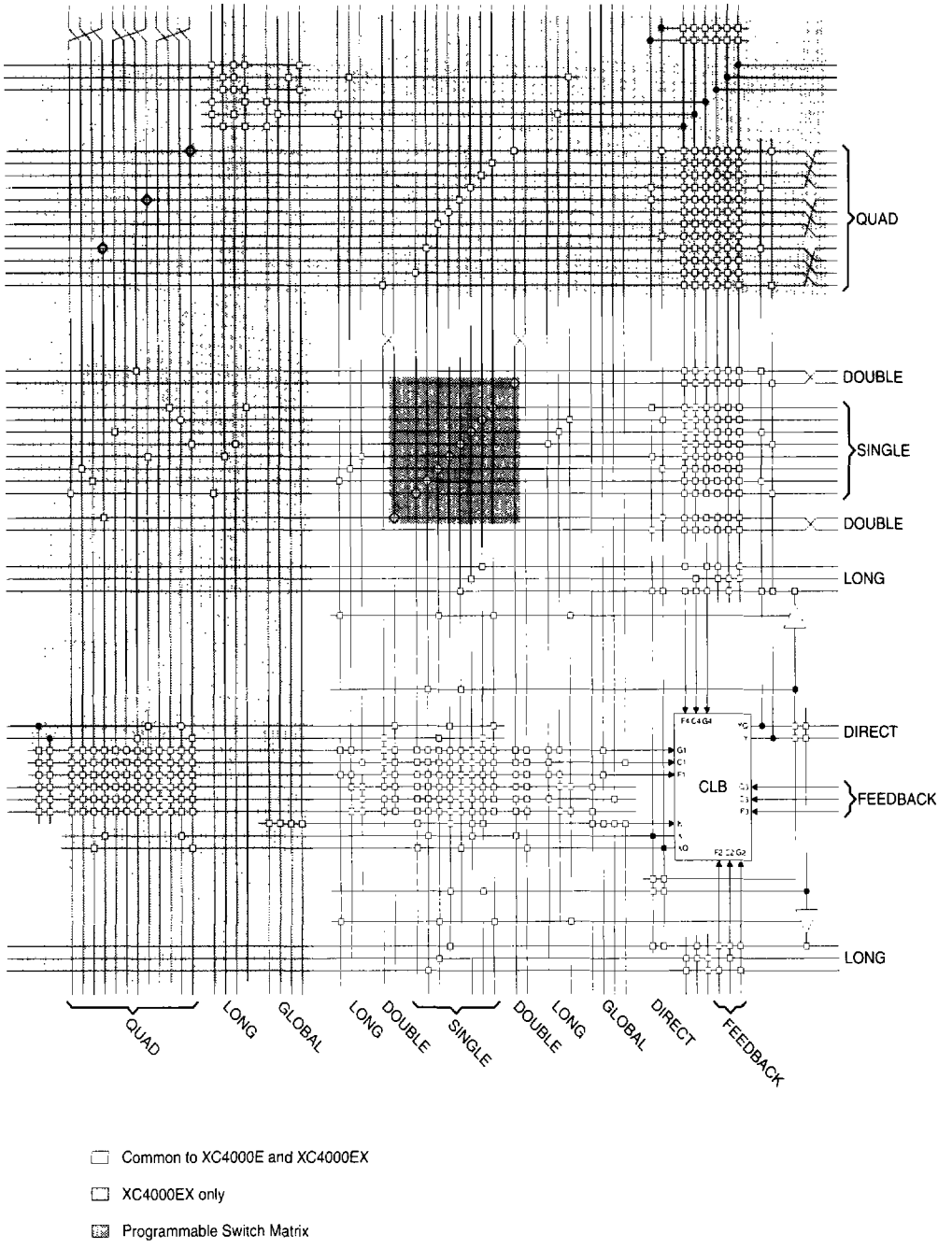


Figure 27: Detail of Programmable Interconnect Associated with XC4000-Series CLB

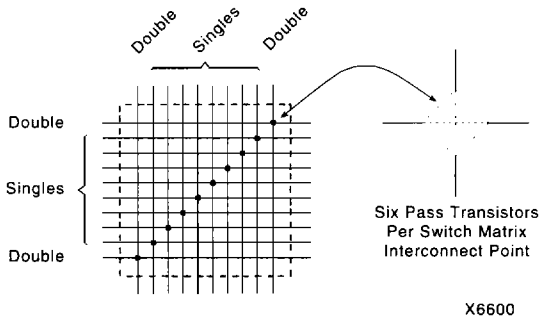


Figure 28: Programmable Switch Matrix (PSM)

Programmable Switch Matrices

The horizontal and vertical single- and double-length lines intersect at a box called a programmable switch matrix (PSM). Each switch matrix consists of programmable pass transistors used to establish connections between the lines (see Figure 28).

For example, a single-length signal entering on the right side of the switch matrix can be routed to a single-length line on the top, left, or bottom sides, or any combination thereof, if multiple branches are required. Similarly, a double-length signal can be routed to a double-length line on any or all of the other three edges of the programmable switch matrix.

Single-Length Lines

Single-length lines provide the greatest interconnect flexibility and offer fast routing between adjacent blocks. There are eight vertical and eight horizontal single-length lines associated with each CLB. These lines connect the switching matrices that are located in every row and a column of CLBs.

Single-length lines are connected by way of the programmable switch matrices, as shown in Figure 29. Routing connectivity is shown in Figure 27.

Single-length lines incur a delay whenever they go through a switching matrix. Therefore, they are not suitable for routing signals for long distances. They are normally used to conduct signals within a localized area and to provide the branching for nets with fanout greater than one.

Double-Length Lines

The double-length lines consist of a grid of metal segments, each twice as long as the single-length lines: they run past two CLBs before entering a switch matrix. Double-length lines are grouped in pairs with the switch matrices staggered, so that each line goes through a switch matrix at every other row or column of CLBs (see Figure 29).

There are four vertical and four horizontal double-length lines associated with each CLB. These lines provide faster signal routing over intermediate distances, while retaining routing flexibility. Double-length lines are connected by way of the programmable switch matrices. Routing connectivity is shown in Figure 27.

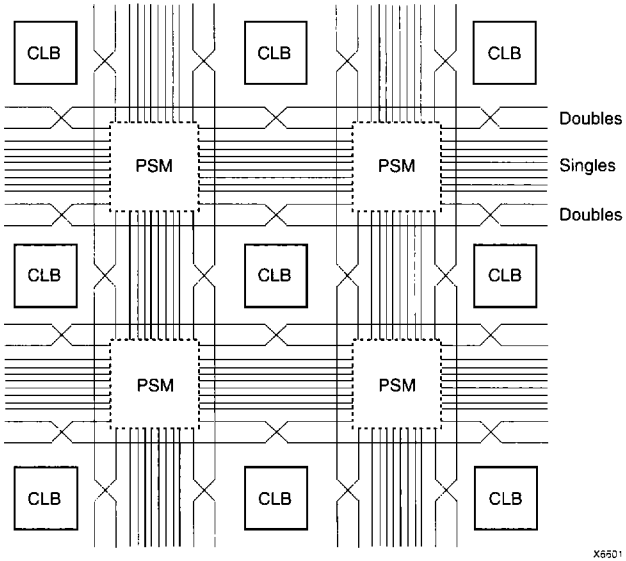


Figure 29: Single- and Double-Length Lines, with Programmable Switch Matrices (PSMs)

Quad Lines (XC4000EX only)

XC4000EX devices also include twelve vertical and twelve horizontal quad lines per CLB row and column. Quad lines are four times as long as the single-length lines. They are interconnected via buffered switch matrices (shown as diamonds in Figure 27 on page 34). Quad lines run past four CLBs before entering a buffered switch matrix. They are grouped in fours, with the buffered switch matrices staggered, so that each line goes through a buffered switch matrix at every fourth CLB location in that row or column. (See Figure 30.)

The buffered switch matrixes have four pins, one on each edge. All of the pins are bidirectional. Any pin can drive any or all of the other pins.

Each buffered switch matrix contains one buffer and six pass transistors. It resembles the programmable switch matrix shown in Figure 28, with the addition of a programmable buffer. There can be up to two independent inputs and up to two independent outputs. Only one of the independent inputs can be buffered.

The place and route software automatically uses the timing requirements of the design to determine whether or not a quad line signal should be buffered. A heavily loaded signal is typically buffered, while a lightly loaded one is not. One scenario is to alternate buffers and pass transistors. This allows both vertical and horizontal quad lines to be buffered at alternating buffered switch matrices.

Due to the buffered switch matrices, quad lines are very fast. They provide the fastest available method of routing heavily loaded signals for long distances across the device.

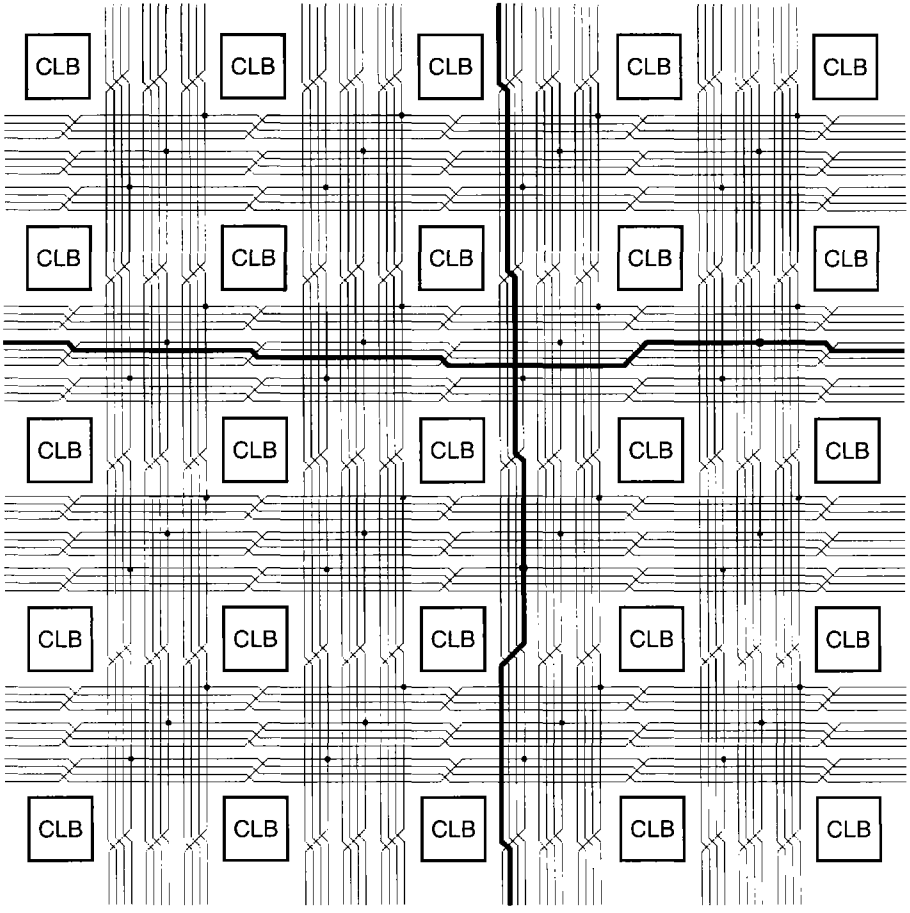


Figure 30: Quad Lines (XC4000EX only)

Longlines

Longlines form a grid of metal interconnect segments that run the entire length or width of the array. Longlines are intended for high fan-out, time-critical signal nets, or nets that are distributed over long distances. In XC4000EX devices, quad lines are preferred for critical nets, because the buffered switch matrices make them faster for high fan-out nets.

Two horizontal longlines per CLB can be driven by 3-state or open-drain drivers (TBUFs). They can therefore implement unidirectional or bidirectional buses, wide multiplexers, or wired-AND functions. (See "Three-State Buffers" on page 29 for more details.)

Each horizontal longline driven by TBUFs has either two (XC4000E) or eight (XC4000EX) pull-up resistors. To activate these resistors, attach a PULLUP symbol to the longline net. The software automatically activates the appropriate number of pull-ups. There is also a weak keeper at each end of these two horizontal longlines. This circuit prevents undefined floating levels. However, it is overridden by any driver, even a pull-up resistor.

Each XC4000E longline has a programmable splitter switch at its center, as does each XC4000EX longline driven by TBUFs. This switch can separate the line into two independent routing channels, each running half the width or height of the array.

Each XC4000EX longline not driven by TBUFs has a buffered programmable splitter switch at the 1/4, 1/2, and 3/4 points of the array. Due to the buffering, XC4000EX longline performance does not deteriorate with the larger array sizes. If the longline is split, the resulting partial longlines are independent.

Routing connectivity of the longlines is shown in Figure 27 on page 34.

Direct Interconnect (XC4000EX only)

The XC4000EX offers two direct, efficient and fast connections between adjacent CLBs. These nets facilitate a data flow from the left to the right side of the device, or from the top to the bottom, as shown in Figure 31. Signals routed on the direct interconnect exhibit minimum interconnect propagation delay and use no general routing resources.

The direct interconnect is also present between CLBs and adjacent IOBs. Each IOB on the left and top device edges has a direct path to the nearest CLB. Each CLB on the right and bottom edges of the array has a direct path to the nearest two IOBs, since there are two IOBs for each row or column of CLBs.

The place and route software uses direct interconnect whenever possible, to maximize routing resources and minimize interconnect delays.

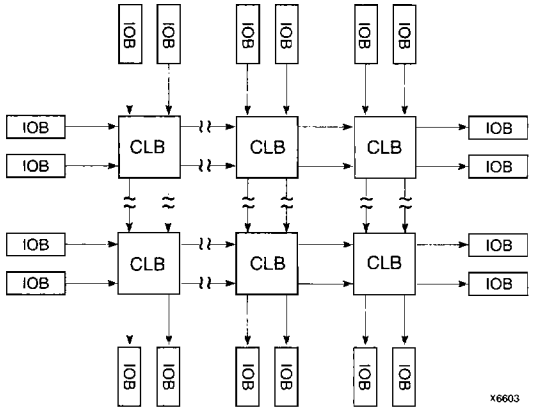


Figure 31: XC4000EX Direct Interconnect

I/O Routing

XC4000-Series devices have additional routing around the IOB ring. This routing is called a VersaRing. The VersaRing facilitates pin-swapping and redesign without affecting board layout. Included are eight double-length lines spanning two CLBs (four IOBs), and four longlines. Global lines and Wide Edge Decoder lines are provided. XC4000EX devices also include eight octal lines.

A high-level diagram of the VersaRing is shown in Figure 32. The shaded arrows represent routing present only in XC4000EX devices.

Figure 33 is a detailed diagram of the XC4000E and XC4000EX VersaRing. The area shown includes two IOBs. There are two IOBs per CLB row or column, therefore this diagram corresponds to the CLB routing diagram shown in Figure 27 on page 34. The shaded areas represent routing and routing connections present only in XC4000EX devices.

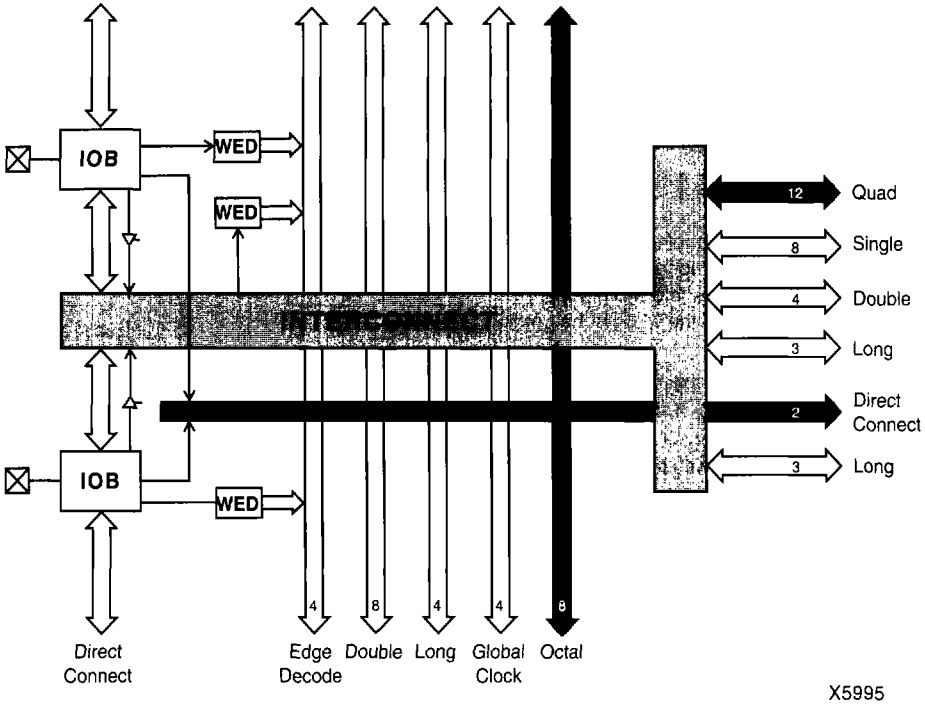


Figure 32: High-Level Routing Diagram of XC4000-Series VersaRing (Left Edge)
WED = Wide Edge Decoder, IOB = I/O Block (shaded arrows indicate XC4000EX only)

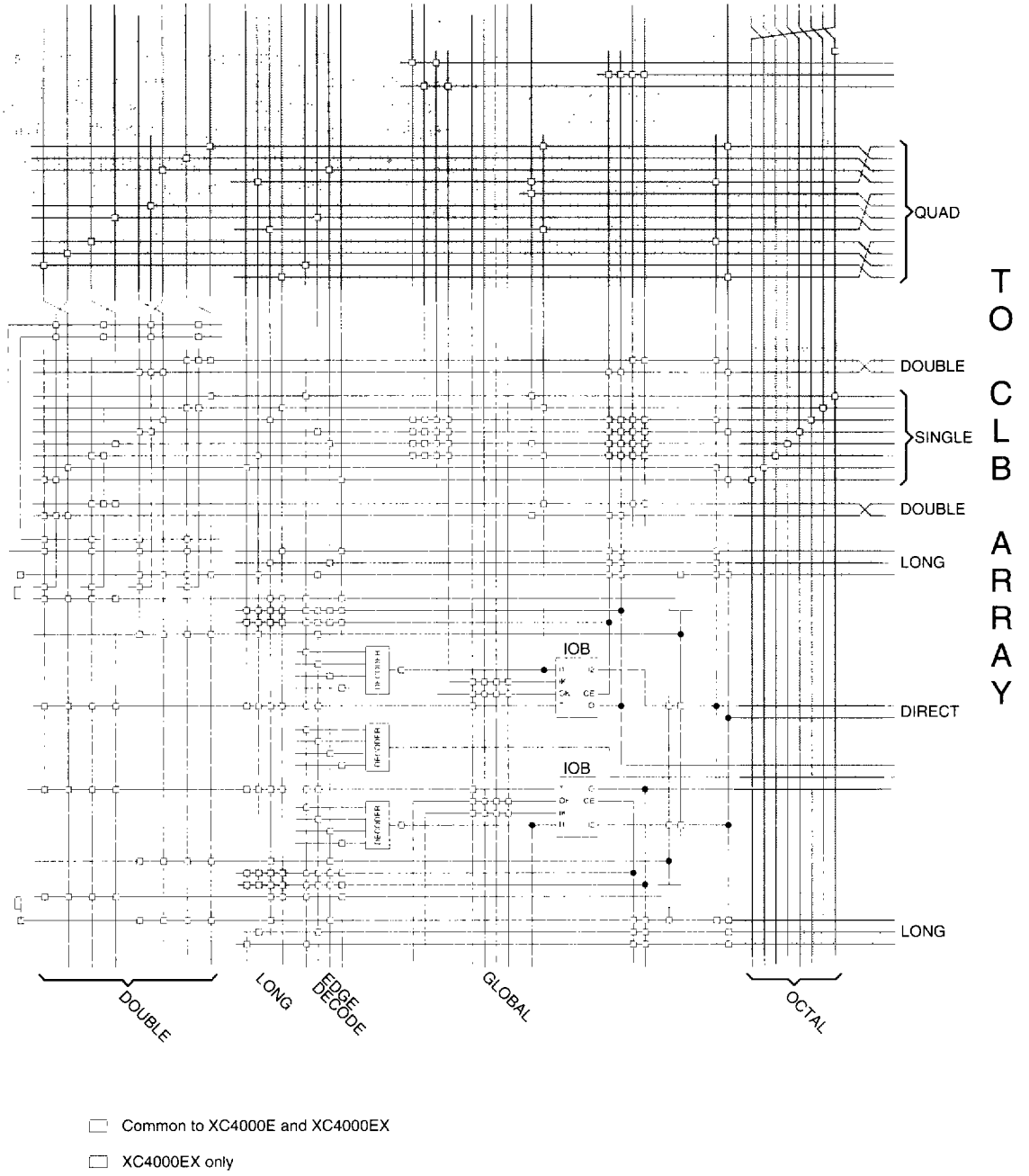


Figure 33: Detail of Programmable Interconnect Associated with XC4000-Series IOB (Left Edge)

Octal I/O Routing (XC4000EX only)

Between the XC4000EX CLB array and the pad ring, eight interconnect tracks provide for versatility in pin assignment and fixed pinout flexibility. (See Figure 34.)

These routing tracks are called octals, because they can be broken every eight CLBs (sixteen IOBs) by a programmable buffer that also functions as a splitter switch. The buffers are staggered, so each line goes through a buffer at every eighth CLB location around the device edge.

The octal lines bend around the corners of the device. The lines cross at the corners in such a way that the segment most recently buffered before the turn has the farthest distance to travel before the next buffer, as shown in Figure 34.

IOB inputs and outputs interface with the octal lines via the single-length interconnect lines. Single-length lines are also used for communication between the octals and double-length lines, quads, and longlines within the CLB array.

Segmentation into buffered octals was found to be optimal for distributing signals over long distances around the device.

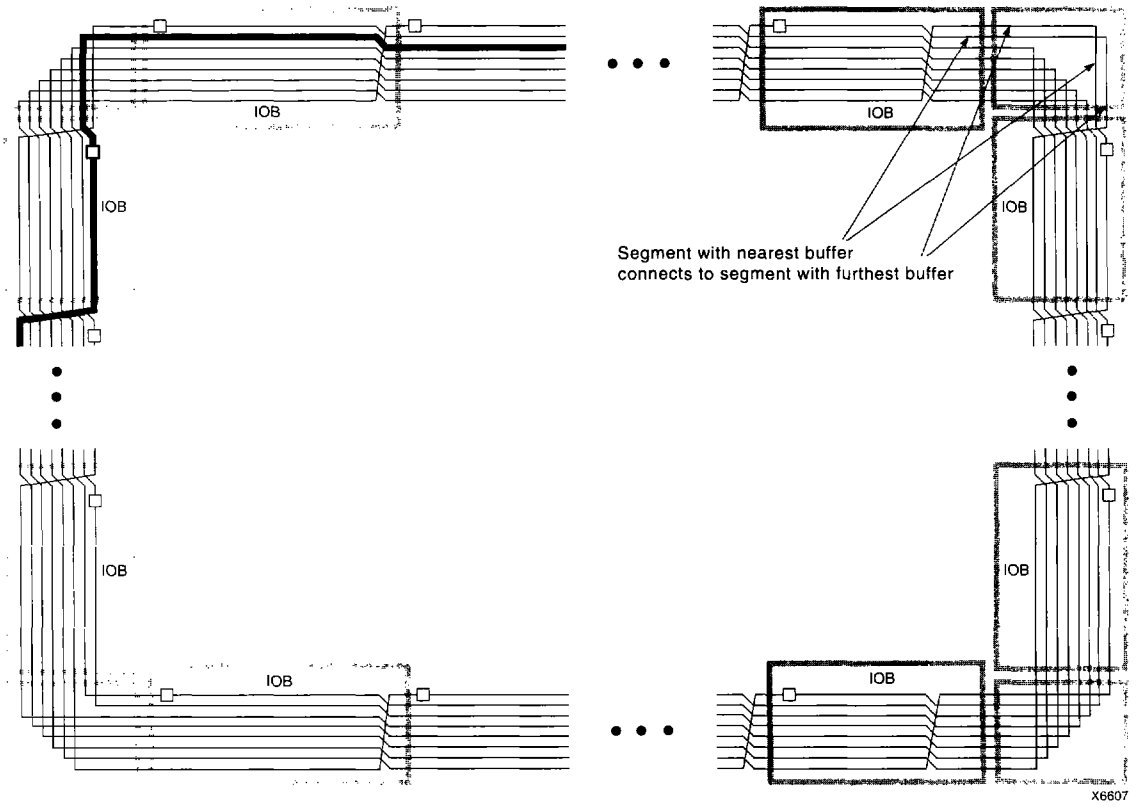


Figure 34: XC4000EX Octal I/O Routing

Global Nets and Buffers

Both the XC4000E and the XC4000EX have dedicated global networks. These networks are designed to distribute clocks and other high fanout control signals throughout the devices with minimal skew. The global buffers are described in detail in the following sections. The text descriptions and diagrams are summarized in Table 17. The table shows which CLB and IOB clock pins can be sourced by which global buffers.

In both XC4000E and XC4000EX devices, placement of a library symbol called BUFG results in the software choosing the appropriate clock buffer, based on the timing requirements of the design. The detailed information in these sections is included only for reference.

Global Nets and Buffers (XC4000E only)

Four vertical longlines in each CLB column are driven exclusively by special global buffers. These longlines are in addition to the vertical longlines used for standard interconnect. The four global lines can be driven by either of two types of global buffers. The clock pins of every CLB and IOB can also be sourced from local interconnect.

Two different types of clock buffers are available in the XC4000E:

- Primary Global Buffers (BUFGP)
- Secondary Global Buffers (BUFGS)

Four Primary Global buffers offer the shortest delay and negligible skew. Four Secondary Global buffers have slightly longer delay and slightly more skew due to potentially heavier loading, but offer greater flexibility when used to drive non-clock CLB inputs.

The Primary Global buffers must be driven by the semi-dedicated pads. The Secondary Global buffers can be sourced by either semi-dedicated pads or internal nets.

Each CLB column has four dedicated vertical Global lines. Each of these lines can be accessed by one particular Primary Global buffer, or by any of the Secondary Global buffers, as shown in Figure 35. Each corner of the device has one Primary buffer and one Secondary buffer.

IOBs along the left and right edges have four vertical global longlines. Top and bottom IOBs can be clocked from the global lines in the adjacent CLB column.

A global buffer should be specified for all timing-sensitive global signal distribution. To use a global buffer, place a BUFGP (primary buffer), BUFGS (secondary buffer), or BUFG (either primary or secondary buffer) element in a schematic or in HDL code. If desired, attach a LOC attribute or property to direct placement to the designated location. For example, attach a LOC=L attribute or property to a BUFGS symbol to direct that a buffer be placed in one of the two Secondary Global buffers on the left edge of the device, or a LOC=BL to indicate the Secondary Global buffer on the bottom edge of the device, on the left.

Table 17: Clock Pin Access

	XC4000E		XC4000EX				Local Interconnect
	BUFGP	BUFGS	BUFGLS	L & R BUFGE	T & B BUFGE	BUFFCLK	
All CLBs in Quadrant	√	√	√	√	√		√
All CLBs in Device	√	√	√				√
IOBs on Adjacent Vertical Half Edge	√	√	√	√	√	√	√
IOBs on Adjacent Vertical Full Edge	√	√	√	√			√
IOBs on Adjacent Horizontal Half Edge (Direct)				√			√
IOBs on Adjacent Horizontal Half Edge (through CLB globals)	√	√	√	√	√		√
IOBs on Adjacent Horizontal Full Edge (through CLB globals)	√	√	√				√

L = Left, R = Right, T = Top, B = Bottom

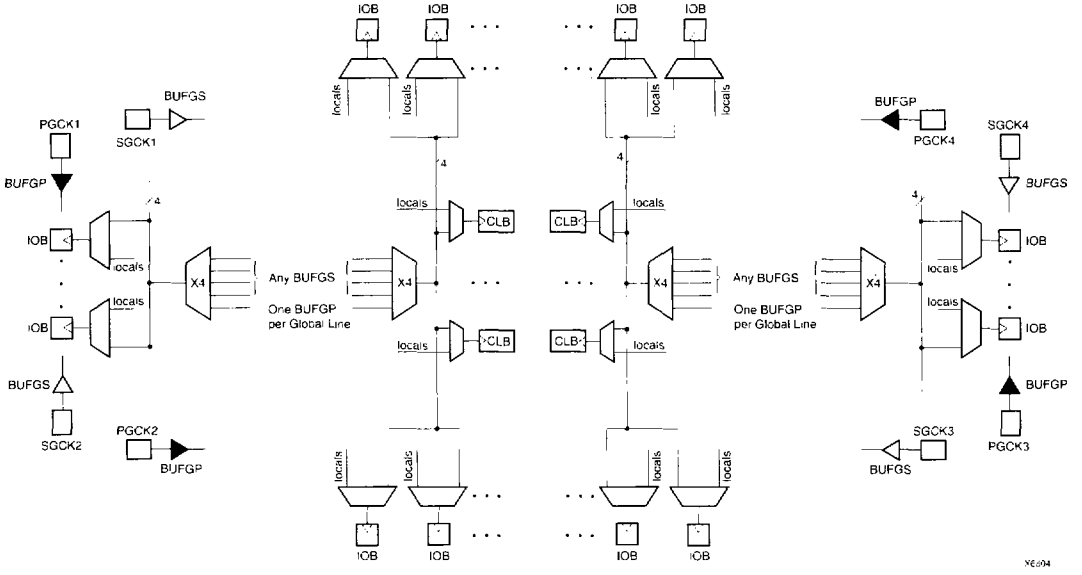


Figure 35: XC4000E Global Net Distribution

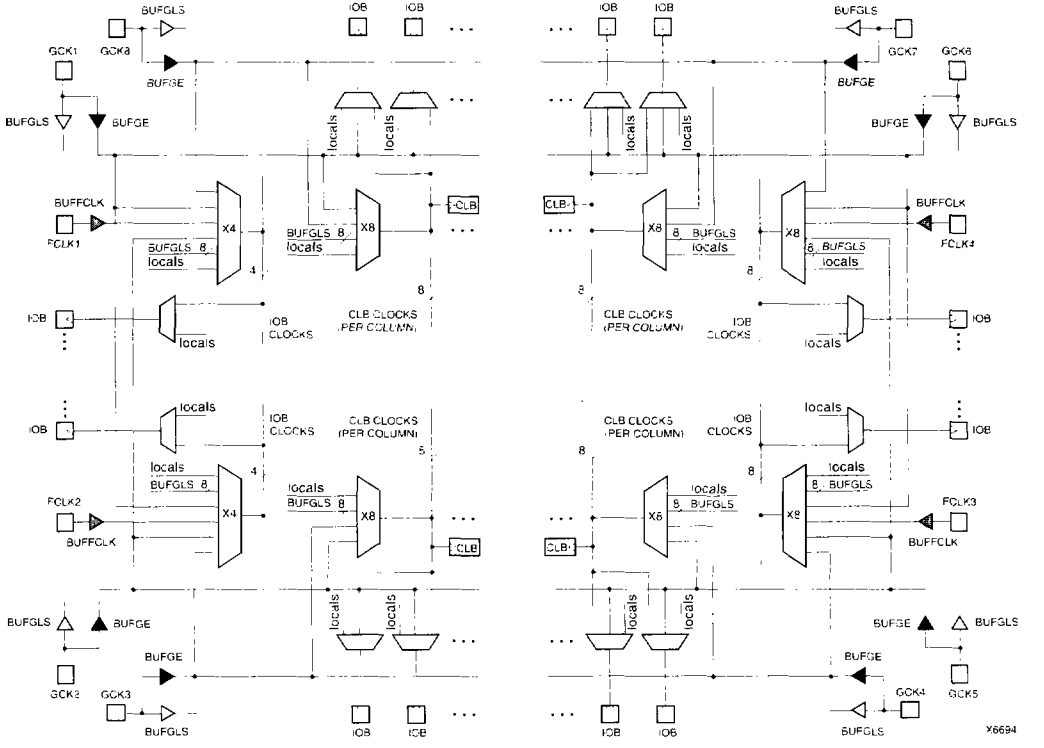


Figure 36: XC4000EX Global Net Distribution

Global Nets and Buffers (XC4000EX only)

Eight vertical longlines in each CLB column are driven by special global buffers. These longlines are in addition to the vertical longlines used for standard interconnect. The global lines are broken in the center of the array, to allow faster distribution and to minimize skew across the whole array. Each half-column global line has its own buffered multiplexer, as shown in Figure 36. The top and bottom global lines cannot be connected across the center of the device, as this connection might introduce unacceptable skew. The top and bottom halves of the global lines must be separately driven — although they can be driven by the same global buffer.

The eight global lines in each CLB column can be driven by either of two types of global buffers. They can also be driven by internal logic, because they can be accessed by single, double, and quad lines at the top, bottom, half, and quarter points. Consequently, the number of different clocks that can be used simultaneously in an XC4000EX device is very large.

There are four global lines feeding the IOBs at the left edge of the device. IOBs along the right edge have eight global lines. There is a single global line along the top and bottom edges with access to the IOBs. All IOB global lines are broken at the center. They cannot be connected across the center of the device, as this connection might introduce unacceptable skew.

IOB global lines can be driven from any of three types of global buffers, or from local interconnect. Alternatively, top and bottom IOBs can be clocked from the global lines in the adjacent CLB column.

Three different types of clock buffers are available in the XC4000EX:

- Global Low-Skew Buffers (BUFGLS)
- Global Early Buffers (BUFGE)
- FastCLK Buffers (BUFFCLK)

Global Low-Skew Buffers are the standard clock buffers. They should be used for most internal clocking, whenever a large portion of the device must be driven.

Global Early Buffers are designed to provide a faster clock access, but CLB access is limited to one-fourth of the device. They also facilitate a faster I/O interface.

FastCLK buffers are specifically designed to provide the fastest possible I/O clock. They have only the standard input access to CLBs, through local interconnect.

Figure 36 is a conceptual diagram of the global net structure in the XC4000EX.

Global Early buffers and Global Low-Skew buffers share a single pad. Therefore, the same IPAD symbol can drive one buffer of each type, in parallel. This configuration is particularly useful when using the Fast Capture latches, as described in "IOB Input Signals" on page 24. Paired Global Early and Global Low-Skew buffers share a common input; they cannot be driven by two different signals.

Choosing an XC4000EX Clock Buffer

The clocking structure of the XC4000EX provides a large variety of features. However, it can be simple to use, without understanding all the details. The software automatically handles clocks, along with all other routing, when the appropriate clock buffer is placed in the design. In fact, if a buffer symbol called BUFG is placed, rather than a specific type of buffer, the software even chooses the buffer most appropriate for the design. The detailed information in this section is provided for those users who want a finer level of control over their designs.

If fine control is desired, use the following summary and Table 17 on page 41 to choose an appropriate clock buffer.

- The simplest thing to do is to use a Global Low-Skew buffer.
- If a faster clock path is needed, try a BUFG. The software will first try to use a Global Low-Skew Buffer. If timing requirements are not met, a faster buffer will automatically be used.
- If a single quadrant of the chip is sufficient for the clocked logic, and the timing requires a faster clock than the Global Low-Skew buffer, use a Global Early buffer.
- In special cases, where both external and internal timing have been carefully studied, a FastCLK buffer can be used, for the fastest possible I/O clock path.

Global Low-Skew Buffers

Each corner of the XC4000EX device has two Global Low-Skew buffers. Any of the eight Global Low-Skew buffers can drive any of the eight vertical Global lines in a column of CLBs. In addition, any of the buffers can drive any of the four vertical lines accessing the IOBs on the left edge of the device, and any of the eight vertical lines accessing the IOBs on the right edge of the device. (See Figure 37 on page 44.)

IOBs at the top and bottom edges of the device are accessed through the vertical Global lines in the CLB array, as in the XC4000E. Any Global Low-Skew buffer can, therefore, access every IOB and CLB in the device.

The Global Low-Skew buffers can be driven by either semi-dedicated pads or internal logic.

To use a Global Low-Skew buffer, place a BUFGLS element in a schematic or in HDL code. If desired, attach a LOC attribute or property to direct placement to the designated location. For example, attach a LOC=T attribute or property to direct that a BUFGLS be placed in one of the two Global Low-Skew buffers on the top edge of the device, or a LOC=TR to indicate the Global Low-Skew buffer on the top edge of the device, on the right.

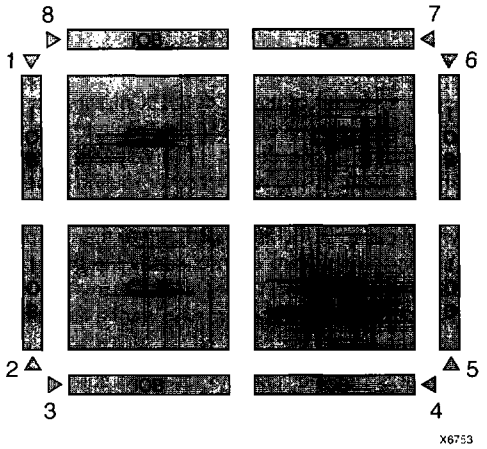


Figure 37: Any BUFGLS (GCK1 - GCK8) Can Drive Any or All Clock Inputs on the Device

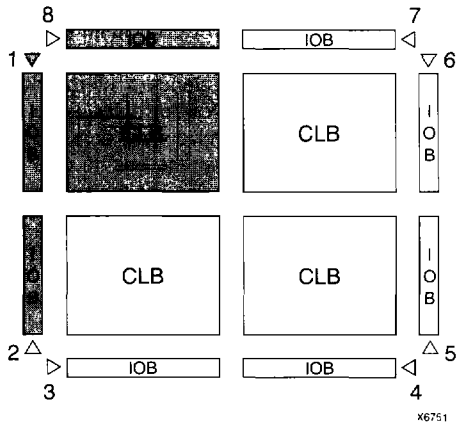


Figure 38: Left and Right BUFGEs Can Drive Any or All Clock Inputs in Same Quadrant or Edge (GCK1 is shown. GCK2, GCK3 and GCK4 are similar.)

Global Early Buffers

Each corner of the XC4000EX device has two Global Early buffers. The primary purpose of the Global Early buffers is to provide an earlier clock access than the potentially heavily-loaded Global Low-Skew buffers. A clock source applied to both buffers will result in the Global Early clock edge occurring several nanoseconds earlier than the Global Low-Skew buffer clock edge, due to the lighter loading.

Global Early buffers also facilitate the fast capture of device inputs, using the Fast Capture latches described in "IOB Input Signals" on page 24. For Fast Capture, take a single clock signal, and route it through both a Global Early buffer and a Global Low-Skew buffer. (The two buffers share an input pad.) Use the Global Early buffer to clock the Fast Capture latch, and the Global Low-Skew buffer to clock the normal input flip-flop or latch, as shown in Figure 18 on page 26.

The Global Early buffers can also be used to provide a fast Clock-to-Out on device output pins. However, an early clock in the output flip-flop IOB must be taken into consideration when calculating the internal clock speed for the design.

The Global Early buffers at the left and right edges of the chip have slightly different capabilities than the ones at the top and bottom. Refer to Figure 38, Figure 39, and Figure 36 on page 42 while reading the following explanation.

Each Global Early buffer can access the eight vertical Global lines for all CLBs in the quadrant. Therefore, only one-fourth of the CLB clock pins can be accessed. This restriction is in large part responsible for the faster speed of the buffers, relative to the Global Low-Skew buffers.

The left-side Global Early buffers can each drive two of the four vertical lines accessing the IOBs on the entire left edge of the device. The right-side Global Early buffers can each drive two of the eight vertical lines accessing the IOBs on the entire right edge of the device. (See Figure 38.)

Each left and right Global Early buffer can also drive half of the IOBs along either the top or bottom edge of the device, using a dedicated line that can only be accessed through the Global Early buffers.

The top and bottom Global Early buffers can drive half of the IOBs along either the left or right edge of the device, as shown in Figure 39. They can only access the top and bottom IOBs via the CLB global lines.

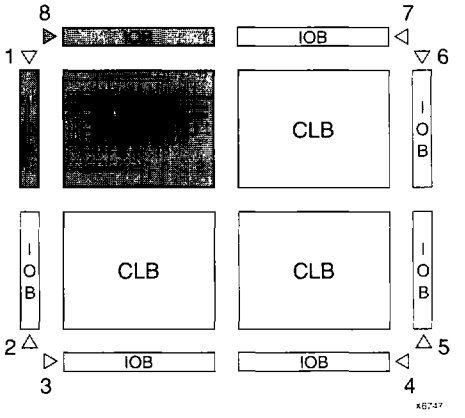


Figure 39: Top and Bottom BUFGEs Can Drive Any or All Clock Inputs in Same Quadrant (GCK8 is shown. GCK3, GCK4 and GCK7 are similar.)

The Global Early buffers can be driven by either semi-dedicated pads or internal logic. They share pads with the Global Low-Skew buffers, so a single net can drive both global buffers, as described above.

To use a Global Early buffer, place a BUFGE element in a schematic or in HDL code. If desired, attach a LOC attribute or property to direct placement to the designated location. For example, attach a LOC=T attribute or property to direct that a BUFGE be placed in one of the two Global Early buffers on the top edge of the device, or a LOC=TR to indicate the Global Early buffer on the top edge of the device, on the right.

FastCLK Buffers

The fastest way to bring a clock into the XC4000EX device is through a FastCLK buffer. Two FastCLK buffers are present on the left edge, and two on the right edge, of the XC4000EX die. There are no FastCLK buffers on the top or bottom edges.

One purpose of the FastCLK buffers is to create a very fast pin-to-pin path by using the IOB 2-input function generator in conjunction with the FastCLK. Drive the F input of the IOB function generator with the FastCLK buffer output, as described in "IOB Output Signals" on page 27.

Alternatively, a FastCLK buffer can be used to minimize the setup time of device inputs, if a positive hold time is acceptable. Use the FastCLK buffer to clock the Fast Capture latch, and a slower clock buffer to clock the standard IOB flip-flop or latch. Either the Global Early buffer or the Global Low-Skew buffer can be used for the second storage element, but whichever one is used should be the same clock as the related internal logic. Since the FastCLK pads are different from the Global Early and Global Low-Skew pads, care must be taken to ensure that skew external to the device does not create internal timing difficulties.

The FastCLK buffers can also be used to provide a fast Clock-to-Out on device output pins. However, a fast clock in the output flip-flop IOB must be taken into consideration when calculating the internal clock speed for the design.

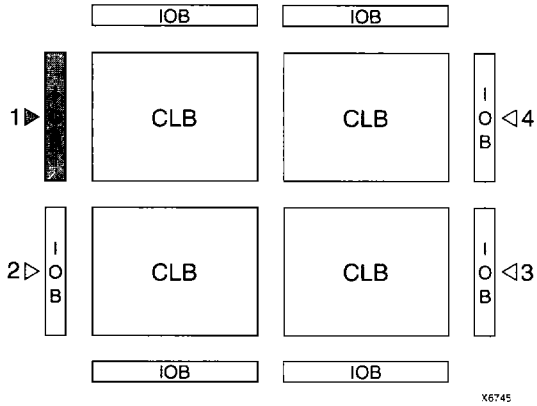


Figure 40: Each BUFFCLK Can Drive Any or All Clock Inputs in Same Half-Edge (FCLK1 is shown. FCLK2, FCLK3 and FCLK4 are similar.)

The FastCLK buffers are limited to accessing IOBs on one-half of the die edge only, as shown in Figure 40 and Figure 36 on page 42. They can each drive two of the four vertical lines accessing the IOBs on the left edge of the device, or two of the eight vertical lines accessing the IOBs on the right edge of the device. They can only access the CLB array through single- and double-length lines.

The FastCLK buffers must be driven by the semi-dedicated IOBs. They are not accessible from internal nets. Other than the FastCLK feature, these IOBs are identical to all other IOBs.

To use a FastCLK buffer, place a BUFFCLK element in a schematic or in HDL code. If desired, attach a LOC attribute or property to direct placement to the designated location. For example, attach a LOC=LB attribute or property to direct that a BUFFCLK be placed on the left edge of the device at the bottom, or use LOC=L to indicate either of the buffers on the left edge.

The input to the BUFFCLK symbol must be driven by a input pad symbol, such as IPAD, or by an input flip-flop or latch, such as INFF, ILD, ILDFFDX, or ILDFLDX.

Power Distribution

Power for the FPGA is distributed through a grid to achieve high noise immunity and isolation between logic and I/O. Inside the FPGA, a dedicated Vcc and Ground ring surrounding the logic array provides power to the I/O drivers, as shown in Figure 41. An independent matrix of Vcc and Ground lines supplies the interior logic of the device.

This power distribution grid provides a stable supply and ground for all internal logic, providing the external package power pins are all connected and appropriately decoupled. Typically, a 0.1 µF capacitor connected near the Vcc and Ground pins of the package will provide adequate decoupling.

Output buffers capable of driving/sinking the specified 12 mA (XC4000E) or 24 mA (XC4000EX) loads under specified worst-case conditions may be capable of driving/sinking up to 10 times as much current under best case conditions.

Noise can be reduced by minimizing external load capacitance and reducing simultaneous output transitions in the same direction. It may also be beneficial to locate heavily loaded output buffers near the Ground pads. The I/O Block output buffers have a slew-rate limited mode (default) which should be used where output rise and fall times are not speed-critical.

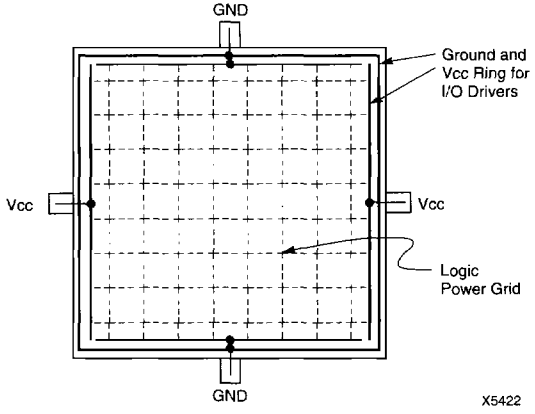


Figure 41: XC4000-Series Power Distribution

Pin Descriptions

There are three types of pins in the XC4000-Series devices:

- Permanently dedicated pins
- User I/O pins that can have special functions
- Unrestricted user-programmable I/O pins.

Before and during configuration, all outputs not used for the configuration process are 3-stated with a 50 kΩ - 100 kΩ pull-up resistor.

After configuration, if an IOB is unused it is configured as an input with a 50 kΩ - 100 kΩ pull-up resistor.

XC4000-Series devices have no dedicated Reset input. Any user I/O can be configured to drive the Global Set/Reset net, GSR. See "Global Set/Reset" on page 13 for more information on GSR.

XC4000-Series devices have no Powerdown control input, as the XC3000 and XC2000 families do. The XC3000/XC2000 Powerdown control also 3-stated all of the device I/O pins. For XC4000-Series devices, use the global 3-state net, GTS, instead. This net 3-states all outputs, but does not place the device in low-power mode. See "IOB Output Signals" on page 27 for more information on GTS.

Device pins for XC4000-Series devices are described in Table 18. Pin functions during configuration for each of the seven configuration modes are summarized in Table 24 on page 78, in the "Configuration Timing" section.

Table 18: Pin Descriptions

Pin Name	I/O During Config.	I/O After Config.	Pin Description
Permanently Dedicated Pins			
VCC	I	I	Eight or more (depending on package) connections to the nominal +5 V supply voltage (+3.3 V for low-voltage devices). All must be connected, and each must be decoupled with a 0.01 - 0.1 µF capacitor to Ground.
GND	I	I	Eight or more (depending on package type) connections to Ground. All must be connected.
CCLK	I or O	I	During configuration, Configuration Clock (CCLK) is an output in Master modes or Asynchronous Peripheral mode, but is an input in Slave mode, Synchronous Peripheral mode, and Express mode. After configuration, CCLK has a weak pull-up resistor and can be selected as the Readback Clock. There is no CCLK High time restriction on XC4000-Series devices, except during Readback. See "Violating the Maximum High and Low Time Specification for the Readback Clock" on page 65 for an explanation of this exception.
DONE	I/O	O	DONE is a bidirectional signal with an optional internal pull-up resistor. As an output, it indicates the completion of the configuration process. As an input, a Low level on DONE can be configured to delay the global logic initialization and the enabling of outputs. The optional pull-up resistor is selected as an option in MakeBits, the XACT*step* program that creates the configuration bitstream. The resistor is included by default.
$\overline{\text{PROGRAM}}$	I	I	$\overline{\text{PROGRAM}}$ is an active Low input that forces the FPGA to clear its configuration memory. It is used to initiate a configuration cycle. When $\overline{\text{PROGRAM}}$ goes High, the FPGA finishes the current clear cycle and executes another complete clear cycle, before it goes into a WAIT state and releases $\overline{\text{INIT}}$. The $\overline{\text{PROGRAM}}$ pin has a permanent weak pull-up, so it need not be externally pulled up to Vcc.
User I/O Pins That Can Have Special Functions			
RDY/$\overline{\text{BUSY}}$	O	I/O	During Peripheral mode configuration, this pin indicates when it is appropriate to write another byte of data into the FPGA. The same status is also available on D7 in Asynchronous Peripheral mode, if a read operation is performed when the device is selected. After configuration, RDY/$\overline{\text{BUSY}}$ is a user-programmable I/O pin. RDY/$\overline{\text{BUSY}}$ is pulled High with a high-impedance pull-up prior to $\overline{\text{INIT}}$ going High.
$\overline{\text{RCLK}}$	O	I/O	During Master Parallel configuration, each change on the A0-A17 outputs (A0 - A21 for XC4000EX) is preceded by a rising edge on $\overline{\text{RCLK}}$, a redundant output signal. $\overline{\text{RCLK}}$ is useful for clocked PROMs. It is rarely used during configuration. After configuration, $\overline{\text{RCLK}}$ is a user-programmable I/O pin.
M0, M1, M2	I	I (M0), O (M1), I (M2)	As Mode inputs, these pins are sampled after $\overline{\text{INIT}}$ goes High to determine the configuration mode to be used. After configuration, M0 and M2 can be used as inputs, and M1 can be used as a 3-state output. These three pins have no associated input or output registers. During configuration, these pins have weak pull-up resistors. For the most popular configuration mode, Slave Serial, the mode pins can thus be left unconnected. The three mode inputs can be individually configured with or without weak pull-up or pull-down resistors. A pull-down resistor value of 4.7 kΩ is recommended. These pins can only be used as inputs or outputs when called out by special schematic definitions. To use these pins, place the library components MD0, MD1, and MD2 instead of the usual pad symbols. Input or output buffers must still be used.

Table 18: Pin Descriptions (Continued)

Pin Name	I/O During Config.	I/O After Config.	Pin Description
TDO	O	O	If boundary scan is used, this pin is the Test Data Output. If boundary scan is not used, this pin is a 3-state output without a register, after configuration is completed. This pin can be user output only when called out by special schematic definitions. To use this pin, place the library component TDO instead of the usual pad symbol. An output buffer must still be used.
TDI, TCK, TMS	I	I/O or I (JTAG)	If boundary scan is used, these pins are Test Data In, Test Clock, and Test Mode Select inputs respectively. They come directly from the pads, bypassing the IOBs. These pins can also be used as inputs to the CLB logic after configuration is completed. If the BSCAN symbol is not placed in the design, all boundary scan functions are inhibited once configuration is completed, and these pins become user-programmable I/O. In this case, they must be called out by special schematic definitions. To use these pins, place the library components TDI, TCK, and TMS instead of the usual pad symbols. Input or output buffers must still be used.
HDC	O	I/O	High During Configuration (HDC) is driven High until the I/O go active. It is available as a control output indicating that configuration is not yet completed. After configuration, HDC is a user-programmable I/O pin.
$\overline{\text{LDC}}$	O	I/O	Low During Configuration ($\overline{\text{LDC}}$) is driven Low until the I/O go active. It is available as a control output indicating that configuration is not yet completed. After configuration, $\overline{\text{LDC}}$ is a user-programmable I/O pin.
$\overline{\text{INIT}}$	I/O	I/O	Before and during configuration, $\overline{\text{INIT}}$ is a bidirectional signal. A 1 kΩ - 10 kΩ external pull-up resistor is recommended. As an active-Low open-drain output, $\overline{\text{INIT}}$ is held Low during the power stabilization and internal clearing of the configuration memory. As an active-Low input, it can be used to hold the FPGA in the internal WAIT state before the start of configuration. Master mode devices stay in a WAIT state an additional 30 to 300 µs after $\overline{\text{INIT}}$ has gone High. During configuration, a Low on this output indicates that a configuration data error has occurred. After the I/O go active, $\overline{\text{INIT}}$ is a user-programmable I/O pin.
PGCK1 - PGCK4 (XC4000E only)	Weak Pull-up	I or I/O	Four Primary Global inputs each drive a dedicated internal global net with short delay and minimal skew. If not used to drive a global buffer, any of these pins is a user-programmable I/O. The PGCK1-PGCK4 pins drive the four Primary Global Buffers. Any input pad symbol connected directly to the input of a BUFGP symbol is automatically placed on one of these pins.
SGCK1 - SGCK4 (XC4000E only)	Weak Pull-up	I or I/O	Four Secondary Global inputs each drive a dedicated internal global net with short delay and minimal skew. These internal global nets can also be driven from internal logic. If not used to drive a global net, any of these pins is a user-programmable I/O pin. The SGCK1-SGCK4 pins provide the shortest path to the four Secondary Global Buffers. Any input pad symbol connected directly to the input of a BUFGS symbol is automatically placed on one of these pins.
GCK1 - GCK8 (XC4000EX only)	Weak Pull-up	I or I/O	Eight inputs can each drive a Global Low-Skew buffer. In addition, each can drive a Global Early buffer. Each pair of global buffers can also be driven from internal logic, but must share an input signal. If not used to drive a global buffer, any of these pins is a user-programmable I/O. Any input pad symbol connected directly to the input of a BUFGLS or BUFGE symbol is automatically placed on one of these pins.
FCLK1 - FCLK4 (XC4000EX only)	Weak Pull-up	I or I/O	Four FCLK inputs can each drive a FastCLK buffer. The FastCLK buffers cannot be driven from internal logic. If not used to drive a global buffer, any of these pins is a user-programmable I/O. Any input pad symbol connected directly to the input of a BUFFCLK symbol is automatically placed on one of these pins.

Table 18: Pin Descriptions (Continued)

Pin Name	I/O During Config.	I/O After Config.	Pin Description
$\overline{CS0}$, CS1, $\overline{WS}$, $\overline{RS}$	I	I/O	These four inputs are used in Asynchronous Peripheral mode. The chip is selected when $\overline{CS0}$ is Low and CS1 is High. While the chip is selected, a Low on Write Strobe ($\overline{WS}$) loads the data present on the D0 - D7 inputs into the internal data buffer. A Low on Read Strobe ($\overline{RS}$) changes D7 into a status output — High if Ready, Low if Busy — and drives D0 - D6 High. In Express mode, CS1 is used as a serial-enable signal for daisy-chaining. $\overline{WS}$ and $\overline{RS}$ should be mutually exclusive, but if both are Low simultaneously, the Write Strobe overrides. After configuration, these are user-programmable I/O pins.
A0 - A17	O	I/O	During Master Parallel configuration, these 18 output pins address the configuration EPROM. After configuration, they are user-programmable I/O pins.
A18 - A21 (XC4000EX only)	O	I/O	During Master Parallel configuration with an XC4000EX master, these 4 output pins add 4 more bits to address the configuration EPROM. After configuration, they are user-programmable I/O pins.
D0 - D7	I	I/O	During Master Parallel and Peripheral configuration, these eight input pins receive configuration data. After configuration, they are user-programmable I/O pins.
DIN	I	I/O	During Slave Serial or Master Serial configuration, DIN is the serial configuration data input receiving data on the rising edge of CCLK. During Parallel configuration, DIN is the D0 input. After configuration, DIN is a user-programmable I/O pin.
DOUT	O	I/O	During configuration in any mode but Express mode, DOUT is the serial configuration data output that can drive the DIN of daisy-chained slave FPGAs. DOUT data changes on the falling edge of CCLK, one-and-a-half CCLK periods after it was received at the DIN input. In Express mode, DOUT is the status output that can drive the CS1 of daisy-chained FPGAs, to enable and disable downstream devices. After configuration, DOUT is a user-programmable I/O pin.
Unrestricted User-Programmable I/O Pins			
I/O	Weak Pull-up	I/O	These pins can be configured to be input and/or output after configuration is completed. Before configuration is completed, these pins have an internal high-value pull-up resistor (50 kΩ - 100 kΩ) that defines the logic level as High.

Boundary Scan

The 'bed of nails' has been the traditional method of testing electronic assemblies. This approach has become less appropriate, due to closer pin spacing and more sophisticated assembly methods like surface-mount technology and multi-layer boards. The IEEE Boundary Scan Standard 1149.1 was developed to facilitate board-level testing of electronic assemblies. Design and test engineers can imbed a standard test logic structure in their device to achieve high fault coverage for I/O and internal logic. This structure is easily implemented with a four-pin interface on any boundary scan-compatible IC. IEEE 1149.1-compatible devices may be serial daisy-chained together, connected in parallel, or a combination of the two.

The XC4000 Series implements IEEE 1149.1-compatible BYPASS, PRELOAD/SAMPLE and EXTEST boundary scan instructions. When the boundary scan configuration option is selected, three normal user I/O pins become dedicated inputs for these functions. Another user output pin becomes the dedicated boundary scan output. The details of how to enable this circuitry are covered later in this section.

By exercising these input signals, the user can serially load commands and data into these devices to control the driving of their outputs and to examine their inputs. This method is an improvement over bed-of-nails testing. It avoids the need to over-drive device outputs, and it reduces the user interface to four pins. An optional fifth pin, a reset for the control logic, is described in the standard but is not implemented in Xilinx devices.

The dedicated on-chip logic implementing the IEEE 1149.1 functions includes a 16-state state machine, an instruction register and a number of data registers. The functional details can be found in the IEEE 1149.1 specification and are also discussed in the Xilinx application note XAPP 017: "*Boundary Scan in XC4000 Devices.*"

Figure 42 shows a simplified block diagram of the XC4000E Input/Output Block with boundary scan implemented. XC4000EX boundary scan logic is identical.

Figure 43 on page 52 is a diagram of the XC4000-Series boundary scan logic. It includes three bits of Data Register per IOB, the IEEE 1149.1 Test Access Port controller, and the Instruction Register with decodes.

XC4000-Series devices can also be configured through the boundary scan logic. See "Configuration Through the Boundary Scan Pins" on page 64.

Data Registers

The primary data register is the boundary scan register. For each IOB pin in the FPGA, bonded or not, it includes three bits for In, Out and 3-State Control. Non-IOB pins have appropriate partial bit population for In or Out only. $\overline{\text{PROGRAM}}$, CCLK and DONE are not included in the boundary scan register. Each EXTEST CAPTURE-DR state captures all In, Out, and 3-state pins.

The data register also includes the following non-pin bits: TDO.T, and TDO.O, which are always bits 0 and 1 of the data register, respectively, and BSCANT.UPD, which is always the last bit of the data register. These three boundary scan bits are special-purpose Xilinx test signals.

The other standard data register is the single flip-flop BYPASS register. It synchronizes data being passed through the FPGA to the next downstream boundary scan device.

The FPGA provides two additional data registers that can be specified using the BSCAN macro. The FPGA provides two user pins (BSCAN.SEL1 and BSCAN.SEL2) which are the decodes of two user instructions. For these instructions, two corresponding pins (BSCAN.TDO1 and BSCAN.TDO2) allow user scan data to be shifted out on TDO. The data register clock (BSCAN.DRCK) is available for control of test logic which the user may wish to implement with CLBs. The NAND of TCK and RUN-TEST-IDLE is also provided (BSCAN.IDLE).

Instruction Set

The XC4000-Series boundary scan instruction set also includes instructions to configure the device and read back the configuration data. The instruction set is coded as shown in Table 19.

Table 19: Boundary Scan Instructions

Instruction			Test Selected	TDO Source	I/O Data Source
I2	I1	I0			
0	0	0	EXTEST	DR	DR
0	0	1	SAMPLE/ PRELOAD	DR	Pin/Logic
0	1	0	USER 1	BSCAN. TDO1	User Logic
0	1	1	USER 2	BSCAN. TDO2	User Logic
1	0	0	READBACK	Readback Data	Pin/Logic
1	0	1	CONFIGURE	DOUT	Disabled
1	1	0	Reserved	—	—
1	1	1	BYPASS	Bypass Register	—

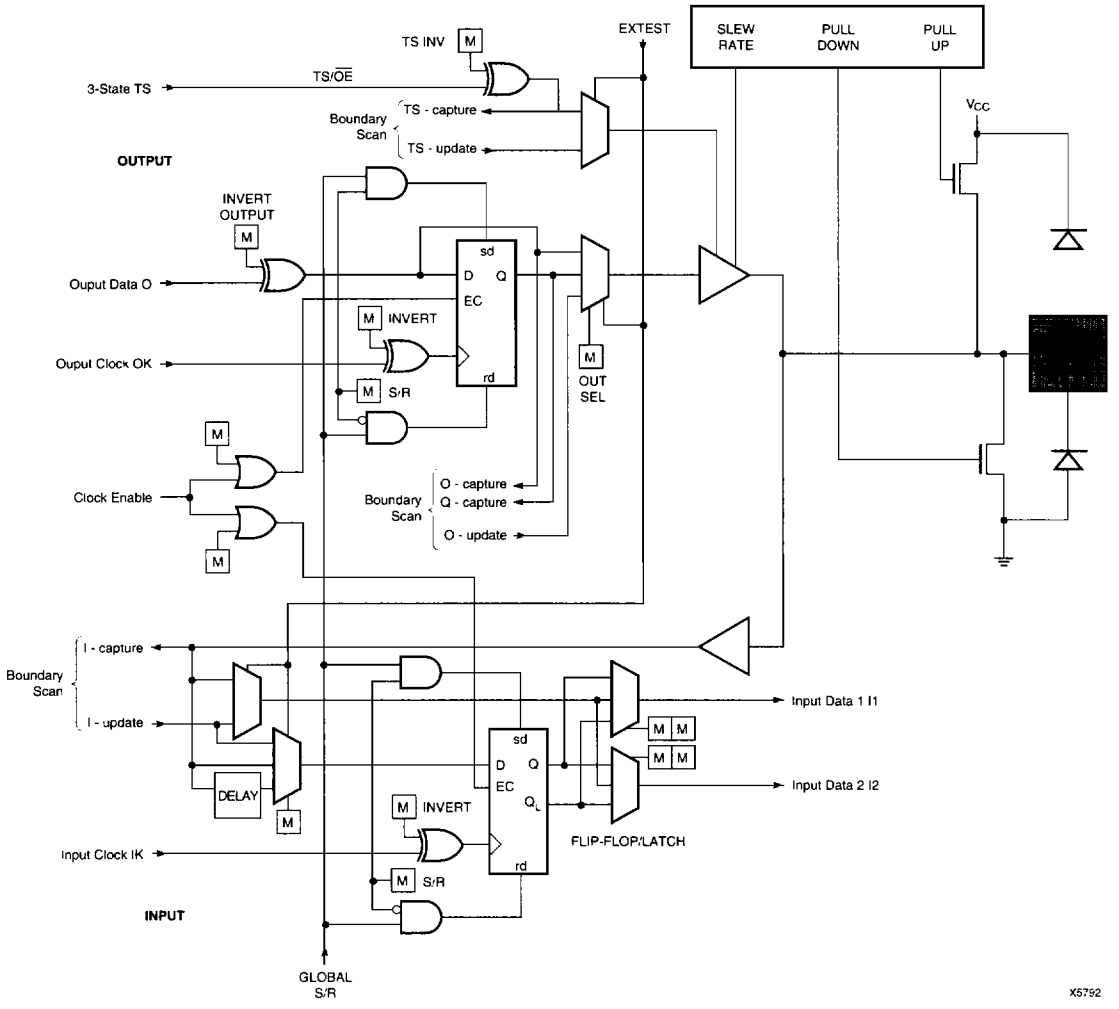


Figure 42: Block Diagram of XC4000E IOB with Boundary Scan (some details not shown). XC4000EX Boundary Scan Logic is Identical.

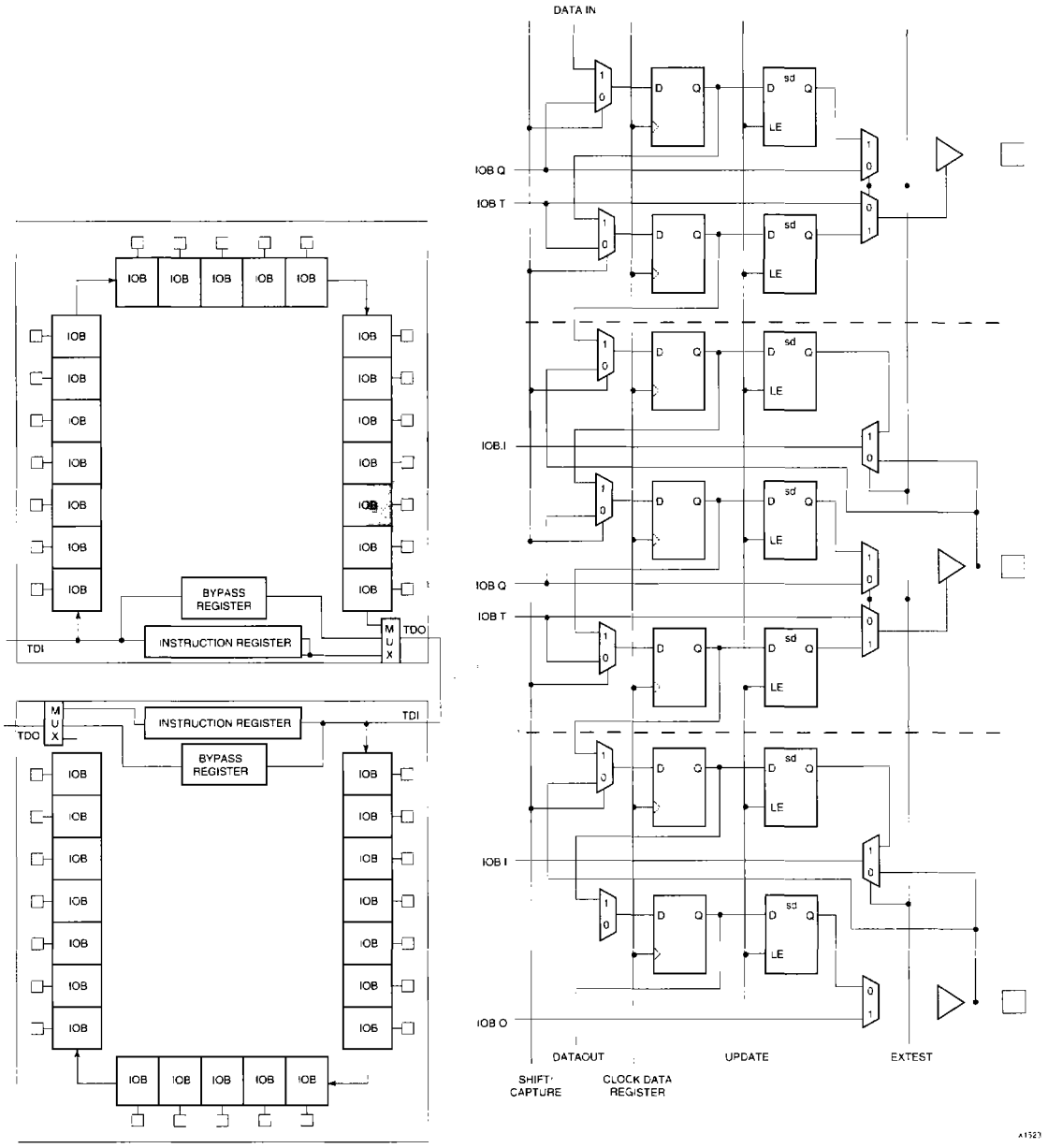


Figure 43: XC4000-Series Boundary Scan Logic

Bit Sequence

The bit sequence within each IOB is: In, Out, 3-State. The input-only M0 and M2 mode pins contribute only the In bit to the boundary scan I/O data register, while the output-only M1 pin contributes all three bits.

The first two bits in the I/O data register are TDO.T and TDO.O, which can be used for the capture of internal signals. The final bit is BSCANT.UPD, which can be used to drive an internal net. These locations are primarily used by Xilinx for internal testing.

From a cavity-up view of the chip (as shown in XDE or Epic), starting in the upper right chip corner, the boundary scan data-register bits are ordered as shown in Figure 44. The device-specific pinout tables for the XC4000 Series include the boundary scan locations for each IOB pin.

BSDL (Boundary Scan Description Language) files for XC4000-Series devices are available on the Xilinx BBS.

Including Boundary Scan in a Schematic

If boundary scan is only to be used during configuration, no special schematic elements need be included in the schematic or HDL code. In this case, the special boundary scan pins TDI, TMS, TCK and TDO can be used for user functions after configuration.

To indicate that boundary scan remain enabled after configuration, place the BSCAN library symbol and connect the TDI, TMS, TCK and TDO pad symbols to the appropriate pins, as shown in Figure 45.

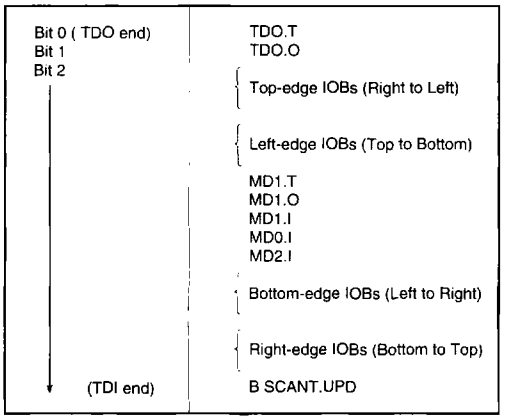


Figure 44: Boundary Scan Bit Sequence

Even if the boundary scan symbol is used in a schematic, the input pins TMS, TCK, and TDI can still be used as inputs to be routed to internal logic. Care must be taken not to force the chip into an undesired boundary scan state by inadvertently applying boundary scan input patterns to these pins. The simplest way to prevent this is to keep TMS High, and then apply whatever signal is desired to TDI and TCK.

Avoiding Inadvertent Boundary Scan Activation

If TMS or TCK is used as user I/O, care must be taken to ensure that at least one of these pins is held constant during configuration. In some applications, a situation may occur where TMS or TCK is driven during configuration. This may cause the device to go into boundary scan mode and disrupt the configuration process.

To prevent activation of boundary scan during configuration, do either of the following:

- TMS: Tie High to put the Test Access Port controller in a benign RESET state
- TCK: Tie High or Low—don't toggle this clock input.

For more information regarding boundary scan, refer to the Xilinx Application Note XAPP 017.001, "*Boundary Scan in XC4000E Devices.*"

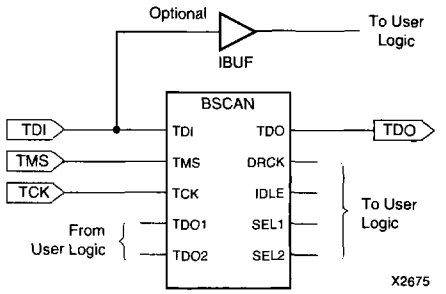


Figure 45: Boundary Scan Schematic Example

Configuration

Configuration is the process of loading design-specific programming data into one or more FPGAs to define the functional operation of the internal blocks and their interconnections. This is somewhat like loading the command registers of a programmable peripheral chip. XC4000-Series devices use several hundred bits of configuration data per CLB and its associated interconnects. Each configuration bit defines the state of a static memory cell that controls either a function look-up table bit, a multiplexer input, or an interconnect pass transistor. The XACT*step* development system translates the design into a netlist file. It automatically partitions, places and routes the logic and generates the configuration data in PROM format.

Special Purpose Pins

Three configuration mode pins (M2, M1, M0) are sampled prior to configuration to determine the configuration mode. After configuration, these pins can be used as auxiliary connections. M2 and M0 can be used as inputs, and M1 can be used as an output. The XACT*step* development system does not use these resources unless they are explicitly specified in the design entry. This is done by placing a special pad symbol called MD2, MD1, or MD0 instead of the input or output pad symbol.

In XC4000-Series devices, the mode pins have weak pull-up resistors during configuration. With all three mode pins High, Slave Serial mode is selected, which is the most popular configuration mode. Therefore, for the most common configuration mode, the mode pins can be left unconnected. (Note, however, that the internal pull-up resistor value can be as high as 100 kΩ.) After configuration, these pins can individually have weak pull-up or pull-down resistors, as specified in the design. A pull-down resistor value of 4.7 kΩ is recommended.

These pins are located in the lower left chip corner and are near the readback nets. This location allows convenient routing if compatibility with the XC2000 and XC3000 family conventions of M0/RT, M1/RD is desired.

Configuration Modes

XC4000E devices have six configuration modes. XC4000EX devices have the same six modes, plus an additional configuration mode. These modes are selected by a 3-bit input code applied to the M2, M1, and M0 inputs. There are three self-loading Master modes, two Peripheral modes, and a Serial Slave mode, which is used primarily for daisy-chained devices. The seventh mode, called Express mode, is an additional slave mode that allows high-speed parallel configuration of the high-capacity XC4000EX devices. The coding for mode selection is shown in Table 20.

Table 20: Configuration Modes

Mode	M2	M1	M0	CCLK	Data
Master Serial	0	0	0	output	Bit-Serial
Slave Serial	1	1	1	input	Bit-Serial
Master Parallel Up	1	0	0	output	Byte-Wide, increment from 00000
Master Parallel Down	1	1	0	output	Byte-Wide, decrement from 3FFFF
Peripheral Synchronous*	0	1	1	input	Byte-Wide
Peripheral Asynchronous	1	0	1	output	Byte-Wide
Express (XC4000EX only)	0	1	0	input	Byte-Wide
Reserved	0	0	1	—	—

Note: * Peripheral Synchronous can be considered byte-wide Slave Parallel

A detailed description of each configuration mode, with timing information, is included later in this data sheet. During configuration, some of the I/O pins are used temporarily for the configuration process. All pins used during configuration are shown in Table 24 on page 78.

Master Modes

The three Master modes use an internal oscillator to generate a Configuration Clock (CCLK) for driving potential slave devices. They also generate address and timing for external PROM(s) containing the configuration data.

Master Parallel (Up or Down) modes generate the CCLK signal and PROM addresses and receive byte parallel data. The data is internally serialized into the FPGA data-frame format. The up and down selection generates starting addresses at either zero or 3FFFF, for compatibility with different microprocessor addressing conventions. The Master Serial mode generates CCLK and receives the configuration data in serial form from a Xilinx serial-configuration PROM.

CCLK speed is selectable as either 1 MHz (default) or 8 MHz (up to 10% lower for low-voltage devices). Configuration always starts at the default slow frequency, then can switch to the higher frequency during the first frame. Frequency tolerance is -50% to +25%.

Peripheral Modes

The two Peripheral modes accept byte-wide data from a bus. A RDY/$\overline{\text{BUSY}}$ status is available as a handshake signal. In Asynchronous Peripheral mode, the internal oscillator generates a CCLK burst signal that serializes the byte-wide data. CCLK can also drive slave devices. In the syn-

chronous mode, an externally supplied clock input to CCLK serializes the data.

Slave Serial Mode

In Slave Serial mode, the FPGA receives serial configuration data on the rising edge of CCLK and, after loading its configuration, passes additional data out, resynchronized on the next falling edge of CCLK.

Multiple slave devices with identical configurations can be wired with parallel DIN inputs. In this way, multiple devices can be configured simultaneously.

Serial Daisy Chain

Multiple devices with different configurations can be connected together in a "daisy chain," and a single combined bitstream used to configure the chain of slave devices.

To configure a daisy chain of devices, wire the CCLK pins of all devices in parallel, as shown in Figure 55 on page 68. Connect the DOUT of each device to the DIN of the next. The lead or master FPGA and following slaves each passes resynchronized configuration data coming from a single source. The header data, including the length count, is passed through and is captured by each FPGA when it recognizes the 0010 preamble. Following the length-count data, each FPGA outputs a High on DOUT until it has received its required number of data frames.

After an FPGA has received its configuration data, it passes on any additional frame start bits and configuration data on DOUT. When the total number of configuration clocks applied after memory initialization equals the value of the 24-bit length count, the FPGAs begin the start-up sequence and become operational together. FPGA I/O are normally released two CCLK cycles after the last configuration bit is received. Figure 49 on page 61 shows the start-up timing for an XC4000-Series device.

The daisy-chained bitstream is not simply a concatenation of the individual bitstreams. The MakePROM program must be used to combine the bitstreams for a daisy-chained configuration.

Multi-Family Daisy Chain

All Xilinx FPGAs of the XC2000, XC3000, and XC4000 Series use a compatible bitstream format and can, therefore, be connected in a daisy chain in an arbitrary sequence. There is, however, one limitation. The lead device must belong to the highest family in the chain. If the chain contains XC4000-Series devices, the master normally cannot be an XC2000 or XC3000 device.

The reason for this rule is shown in Figure 49 on page 61. Since all devices in the chain store the same length count value and generate or receive one common sequence of CCLK pulses, they all recognize length-count match on the same CCLK edge, as indicated on the left edge of Figure 49. The master device then generates additional CCLK pulses until it reaches its finish point F. The different families generate or require different numbers of additional CCLK pulses until they reach F. Not reaching F means that the device does not really finish its configuration, although DONE may have gone High, the outputs became active, and the internal reset was released. For the XC4000-Series device, not reaching F means that readback cannot be initiated and most boundary scan instructions cannot be used.

The user has some control over the relative timing of these events and can, therefore, make sure that they occur at the proper time and the finish point F is reached. Timing is controlled using MakeBits options.

XC3000 Master with an XC4000-Series Slave

Some designers want to use an inexpensive lead device in peripheral mode and have the more precious I/O pins of the XC4000-Series devices all available for user I/O. Figure 46 provides a solution for that case.

This solution requires one CLB, one IOB and pin, and an internal oscillator with a frequency of up to 5 MHz as a clock source. The XC3000 master device must be configured with late Internal Reset, which is the default option.

One CLB and one IOB in the lead XC3000-family device are used to generate the additional CCLK pulse required by the XC4000-Series devices. When the lead device removes the internal RESET signal, the 2-bit shift register responds to its clock input and generates an active Low output signal for the duration of the subsequent clock period. An external connection between this output and CCLK thus creates the extra CCLK pulse.

Express Mode (XC4000EX only)

Express mode is similar to Slave Serial mode, except the data is presented in parallel format, and is clocked into the target device a byte at a time rather than a bit at a time. The data is loaded in parallel into eight different columns: it is not internally serialized. Eight bits of configuration data are loaded with every CCLK cycle, therefore this configuration

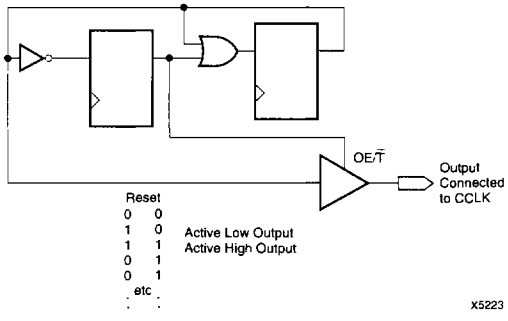


Figure 46: CCLK Generation for XC3000 Master Driving an XC4000-Series Slave

mode runs at eight times the data rate of the other six modes. A length count is not used in Express mode.

Express mode must be specified as an option to the MakeBits program, which generates the bitstream. The Express mode bitstream is not compatible with the other six configuration modes.

Multiple slave devices with identical configurations can be wired with parallel D0-D7 inputs. In this way, multiple devices can be configured simultaneously.

Pseudo Daisy Chain

Multiple devices with different configurations can be connected together in a pseudo daisy chain, provided that all of the devices are in Express mode. A single combined bitstream is used to configure the chain of Express mode devices, but the input data bus must drive D0-D7 of each device. Tie High the CS1 pin of the first device to be configured. Connect the DOUT pin of each FPGA to the CS1 pin of the next device in the chain. The D0-D7 inputs are wired to each device in parallel. The DONE pins are wired together, with one or more internal DONE pull-ups activated. Alternatively, a 4.7 kΩ external resistor can be used, if desired. (See Figure 63 on page 76.)

The requirement that all DONE pins in a daisy chain be wired together applies only to Express mode, and only if all devices in the chain are to become active simultaneously. All XC4000EX devices in Express mode are synchronized to the DONE pin. User I/O for each device become active after the DONE pin for that device goes High. (The exact timing is determined by MakeBits options.) Since the DONE pin is open-drain and does not drive a High value, tying the DONE pins of all devices together prevents all devices in the chain from going High until the last device in the chain has completed its configuration cycle.

Because only XC4000EX and XC5200 devices support Express mode, only these devices can be used to form an Express mode daisy chain. XC5200 devices used in a combined daisy chain with XC4000EX devices should be configured as synchronized to DONE (MakeBits option CCLK_SYNC or UCLK_SYNC), and their DONE pins wired together with those of the XC4000EX devices.

Setting CCLK Frequency

For Master modes, CCLK can be generated in either of two frequencies. In the default slow mode, the frequency ranges from 0.5 MHz to 1.25 MHz (up to 10% lower for low-voltage devices). In fast CCLK mode, the frequency ranges from 4 MHz to 10 MHz (up to 10% lower for low-voltage devices). The frequency is selected by an option when running MakeBits, the bitstream generation software tool. If an XC4000-Series Master is driving an XC3000- or XC2000-family slave, slow CCLK mode must be used. Slow mode is the default.

Data Stream Format

The data stream ("bitstream") format is identical for all configuration modes, with the exception of Express mode. In Express mode, the device becomes active when DONE goes High, therefore no length count is required. Additionally, CRC error checking is not supported in Express mode.

The data stream formats are shown in Table 21. Express mode data is shown with D0 at the left and D7 at the right. For all other modes, bit-serial data is read from left to right, and byte-parallel data is effectively assembled from this serial bitstream, with the first bit in each byte assigned to D0.

The configuration data stream begins with a string of eight ones, a preamble code, followed by a 24-bit length count and a separator field of ones (or 24 fill bits, in Express mode). This header is followed by the actual configuration data in frames. The length and number of frames depends on the device type (see Table 22 and Table 23). Each frame begins with a start field and ends with an error check. In all modes except Express mode, a postamble code is required to signal the end of data for a single device. In all cases, additional start-up bytes of data are required to provide four clocks for the startup sequence at the end of configuration. Long daisy chains require additional startup bytes to shift the last data through the chain. All startup bytes are don't-cares; these bytes are not included in bitstreams created by the Xilinx software.

Table 21: XC4000-Series Data Stream Formats

Data Type	Express Mode (D0-D7)	All Other Modes (D0...)
Fill Byte	11111111b	11111111b
Preamble Code	11110010b	0010b
Length Count	FFFFFFh	COUNT(23:0)
Fill Bits	—	1111b
Start Field	11010010b	0b
Data Frame	DATA(n-1:0)	DATA(n-1:0)
CRC or Constant Field Check	11010010b	xxxx (CRC) or 0110b
Extend Write Cycle	FFFFFFFFFFh	—
Postamble	—	01111111b
Start-Up Bytes	xxxxxxxxh	xxh

LEGEND:

Unshaded	Once per bitstream
Light	Once per data frame
Dark	Once per device

Table 22: XC4000E Program Data

Device	XC4003E	XC4005E/L	XC4006E	XC4008E	XC4010E/L	XC4013E/L	XC4020E	XC4025E
Max Logic Gates	3,000	5,000	6,000	8,000	10,000	13,000	20,000	25,000
CLBs (Row x Col.)	100 (10 x 10)	196 (14 x 14)	256 (16 x 16)	324 (18 x 18)	400 (20 x 20)	576 (24 x 24)	784 (28 x 28)	1,024 (32 x 32)
IOBs	80	112	128	144	160	192	224	256
Flip-Flops	360	616	768	936	1,120	1,536	2,016	2,560
Horizontal Longlines	20	28	32	36	40	48	56	64
TBUFs per Longline	12	16	18	20	22	26	30	34
Bits per Frame	126	166	186	206	226	266	306	346
Frames	428	572	644	716	788	932	1,076	1,220
Program Data	53,936	94,960	119,792	147,504	178,096	247,920	329,264	422,128
PROM Size (bits)	53,976	95,000	119,832	147,544	178,136	247,960	329,304	422,168

Notes: 1. Bits per Frame = (10 x number of rows) + 7 for the top + 13 for the bottom + 1 + 1 start bit + 4 error check bits
Number of Frames = (36 x number of columns) + 26 for the left edge + 41 for the right edge + 1
Program Data = (Bits per Frame x Number of Frames) + 8 postamble bits
PROM Size = Program Data + 40

2. The user can add more "one" bits as leading dummy bits in the header, or, if CRC = off, as trailing dummy bits at the end of any frame, following the four error check bits. However, the Length Count value **must** be adjusted for all such extra "one" bits, even for extra leading ones at the beginning of the header.

The MakeBits software creates the configuration bitstream. In Express mode, only non-CRC error checking is supported. In all other modes, MakeBits allows a selection of CRC or non-CRC error checking. The non-CRC error checking tests for a designated end-of-frame field for each frame. For CRC error checking, MakeBits calculates a running CRC and inserts a unique four-bit partial check at the end of each frame. The 11-bit CRC check of the last frame of an FPGA includes the last seven data bits.

Detection of an error results in the suspension of data loading and the pulling down of the $\overline{\text{INIT}}$ pin. In Master modes, CCLK and address signals continue to operate externally. The user must detect $\overline{\text{INIT}}$ and initialize a new configuration by pulsing the $\overline{\text{PROGRAM}}$ pin Low or cycling Vcc.

Cyclic Redundancy Check (CRC) for Configuration and Readback

The Cyclic Redundancy Check is a method of error detection in data transmission applications. Generally, the transmitting system performs a calculation on the serial bitstream. The result of this calculation is tagged onto the data stream as additional check bits. The receiving system performs an identical calculation on the bitstream and compares the result with the received checksum.

Each data frame of the configuration bitstream has four error bits at the end, as shown in Table 21. If a frame data error is detected during the loading of the FPGA, the configuration process with a potentially corrupted bitstream is terminated. The FPGA pulls the $\overline{\text{INIT}}$ pin Low and goes into a Wait state.

During Readback, 11 bits of the 16-bit checksum are added to the end of the Readback data stream. The checksum is computed using the CRC-16 CCITT polynomial, as shown in Figure 47. The checksum consists of the 11 most significant bits of the 16-bit code. A change in the checksum indicates a change in the Readback bitstream. A comparison to a previous checksum is meaningful only if the readback data is independent of the current device state. CLB outputs should not be included (Read Capture MakeBits option not used), and if RAM is present, the RAM content must be unchanged.

Statistically, one error out of 2048 might go undetected.

Table 23: XC4000EX Program Data

Device	XC4028EX/XL	XC4036EX/XL	XC4044EX/XL	XC4052XL	XC4062XL
Max Logic Gates	28,000	36,000	44,000	52,000	62,000
CLBs (Row x Col.)	1,024 (32 x 32)	1,296 (36 x 36)	1,600 (40 x 40)	1,936 (44 x 44)	2,304 (48 x 48)
IOBs	256	288	320	352	384
Flip-Flops	2,560	3,168	3,840	4,576	5,376
Horizontal Longlines	192	216	240	264	288
TBUFs per Longline	34	38	42	46	50
Bits per Frame	421	469	517	565	613
Frames	1587	1775	1963	2151	2,339
Program Data	668,127	832,483	1,014,879	1,215,323	1,433,807
PROM Size (bits)	668,167	832,523	1,014,919	1,215,363	1,433,847

Notes:
1. Bits per Frame = (12 x number of rows) + 8 for the top + 16 for the bottom + 8 + 1 start bit + 4 error check bits
   Number of Frames = (47 x number of columns) + 27 for the left edge + 52 for the right edge + 4
   Program Data = (Bits per Frame x Number of Frames) + 8 postamble bits
   PROM Size = Program Data + 40
2. The user can add more "one" bits as leading dummy bits in the header, or, if CRC = off, as trailing dummy bits at the end of any frame, following the four error check bits. However, the Length Count value **must** be adjusted for all such extra "one" bits, even for extra leading ones at the beginning of the header.
3. Express mode bitfiles are slightly larger (see Table 21).

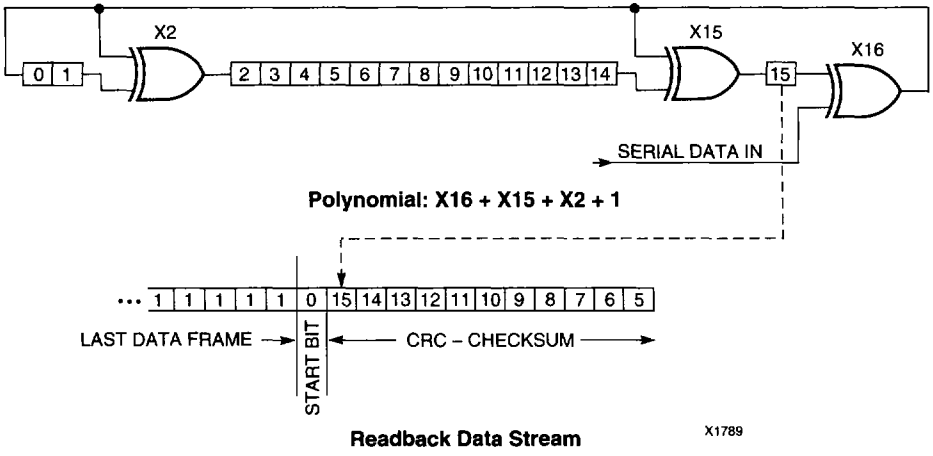


Figure 47: Circuit for Generating CRC-16

Configuration Sequence

There are four major steps in the XC4000-Series power-up configuration sequence.

- Configuration Memory Clear
- Initialization
- Configuration
- Start-Up

The full process is illustrated in Figure 48.

Configuration Memory Clear

When power is first applied or is reapplied to an FPGA, an internal circuit forces initialization of the configuration logic. When Vcc reaches an operational level, and the circuit passes the write and read test of a sample pair of configuration bits, a time delay is started. This time delay is nominally 16 ms, and up to 10% longer in the low-voltage devices. The delay is four times as long when in Master Modes (M0 Low), to allow ample time for all slaves to reach a stable Vcc. When all $\overline{INIT}$ pins are tied together, as recommended, the longest delay takes precedence. Therefore, devices with different time delays can easily be mixed and matched in a daisy chain.

This delay is applied only on power-up. It is not applied when reconfiguring an FPGA by pulsing the $\overline{PROGRAM}$ pin Low. During this time delay, or as long as the $\overline{PROGRAM}$ input is asserted, the configuration logic is held in a Configuration Memory Clear state. The configuration-memory frames are consecutively initialized, using the internal oscillator.

At the end of each complete pass through the frame addressing, the power-on time-out delay circuitry and the level of the $\overline{PROGRAM}$ pin are tested. If neither is asserted, the logic initiates one additional clearing of the configuration frames and then tests the $\overline{INIT}$ input.

Initialization

During initialization and configuration, user pins HDC, $\overline{LDC}$, $\overline{INIT}$ and DONE provide status outputs for the system interface. The outputs $\overline{LDC}$, $\overline{INIT}$ and DONE are held Low and HDC is held High starting at the initial application of power.

The open drain $\overline{INIT}$ pin is released after the final initialization pass through the frame addresses. There is a deliberate delay of 50 to 250 µs (up to 10% longer for low-voltage devices) before a Master-mode device recognizes an inactive $\overline{INIT}$. Two internal clocks after the $\overline{INIT}$ pin is recognized as High, the FPGA samples the three mode lines to determine the configuration mode. The appropriate interface lines become active and the configuration preamble and data can be loaded.

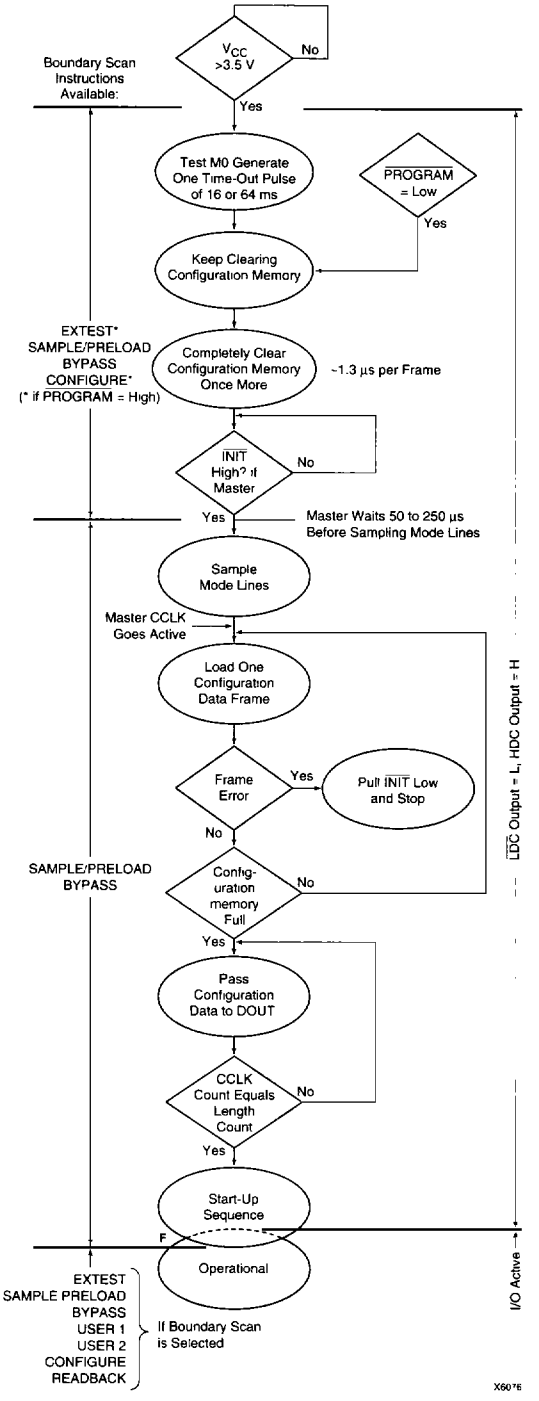


Figure 48: Power-up Configuration Sequence

Configuration

The 0010 preamble code, included for all modes except Express mode, indicates that the following 24 bits represent the length count. The length count is the total number of configuration clocks needed to load the complete configuration data. (Four additional configuration clocks are required to complete the configuration process, as discussed below.) After the preamble and the length count have been passed through to all devices in the daisy chain, DOUT is held High to prevent frame start bits from reaching any daisy-chained devices. In Express mode, the length count bits are ignored, and DOUT is held Low, to disable the next device in the pseudo daisy chain.

A specific configuration bit, early in the first frame of a master device, controls the configuration-clock rate and can increase it by a factor of eight. Therefore, if a fast configuration clock is selected by the bitstream, the slower clock rate is used until this configuration bit is detected.

Each frame has a start field followed by the frame-configuration data bits and a frame error field. If a frame data error is detected, the FPGA halts loading, and signals the error by pulling the open-drain $\overline{INIT}$ pin Low. After all configuration frames have been loaded into an FPGA, DOUT again follows the input data so that the remaining data is passed on to the next device. In Express mode, when the first device is fully programmed, DOUT goes High to enable the next device in the chain.

Delaying Configuration After Power-Up

There are two methods of delaying configuration after power-up: put a logic Low on the $\overline{PROGRAM}$ input, or pull the bidirectional $\overline{INIT}$ pin Low, using an open-collector (open-drain) driver. (See Figure 48 on page 59.)

A Low on the $\overline{PROGRAM}$ input is the more radical approach, and is recommended when the power-supply rise time is excessive or poorly defined. As long as $\overline{PROGRAM}$ is Low, the FPGA keeps clearing its configuration memory. When $\overline{PROGRAM}$ goes High, the configuration memory is cleared one more time, followed by the beginning of configuration, provided the $\overline{INIT}$ input is not externally held Low. Note that a Low on the $\overline{PROGRAM}$ input automatically forces a Low on the $\overline{INIT}$ output. The XC4000-Series $\overline{PROGRAM}$ pin has a permanent weak pull-up.

Using an open-collector or open-drain driver to hold $\overline{INIT}$ Low before the beginning of configuration causes the FPGA to wait after completing the configuration memory clear operation. When $\overline{INIT}$ is no longer held Low externally, the device determines its configuration mode by capturing its mode pins, and is ready to start the configuration process. A master device waits up to an additional 250 µs to make sure that any slaves in the optional daisy chain have seen that $\overline{INIT}$ is High.

Start-Up

Start-up is the transition from the configuration process to the intended user operation. This transition involves a change from one clock source to another, and a change from interfacing parallel or serial configuration data where most outputs are 3-stated, to normal operation with I/O pins active in the user-system. Start-up must make sure that the user-logic 'wakes up' gracefully, that the outputs become active without causing contention with the configuration signals, and that the internal flip-flops are released from the global Reset or Set at the right time.

Figure 49 describes start-up timing for the three Xilinx families in detail. Express mode configuration always uses either CCLK_SYNC or UCLK_SYNC timing, the other configuration modes can use any of the four timing sequences.

To access the internal start-up signals, place the STARTUP library symbol.

Start-up Timing

Different FPGA families have different start-up sequences.

The XC2000 family goes through a fixed sequence. DONE goes High and the internal global Reset is de-activated one CCLK period after the I/O become active.

The XC3000A family offers some flexibility. DONE can be programmed to go High one CCLK period before or after the I/O become active. Independent of DONE, the internal global Reset is de-activated one CCLK period before or after the I/O become active.

The XC4000 Series offers additional flexibility. The three events — DONE going High, the internal Set/Reset being de-activated, and the user I/O going active — can all occur in any arbitrary sequence. Each of them can occur one CCLK period before or after, or simultaneous with, any of the others. This relative timing is selected by means of software options in MakeBits, the bitstream generation software.

The default option, and the most practical one, is for DONE to go High first, disconnecting the configuration data source and avoiding any contention when the I/Os become active one clock later. Reset/Set is then released another clock period later to make sure that user-operation starts from stable internal conditions. This is the most common sequence, shown with heavy lines in Figure 49, but the designer can modify it to meet particular requirements.

Normally, the start-up sequence is controlled by the internal device oscillator output (CCLK), which is asynchronous to the system clock.

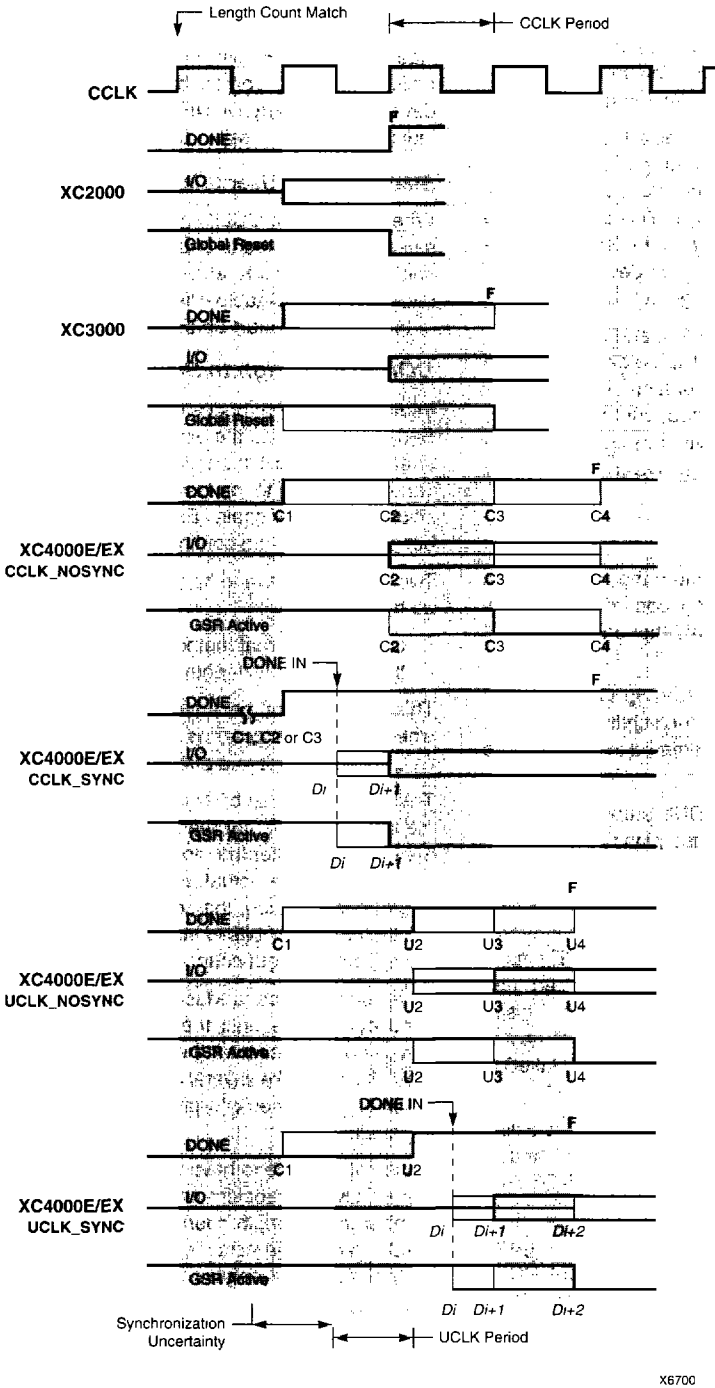


Figure 49: Start-up Timing

The XC4000 Series offers another start-up clocking option, UCLK_NOSYNC. The three events described above need not be triggered by CCLK. They can, as a configuration option, be triggered by a user clock. This means that the device can wake up in synchronism with the user system.

When the UCLK_SYNC option is enabled, the user can externally hold the open-drain DONE output Low, and thus stall all further progress in the start-up sequence until DONE is released and has gone High. This option can be used to force synchronization of several FPGAs to a common user clock, or to guarantee that all devices are successfully configured before any I/Os go active.

If either of these two options is selected, and no user clock is specified in the design or attached to the device, the chip could reach a point where the configuration of the device is complete and the Done pin is asserted, but the outputs do not become active. The solution is either to recreate the bitstream specifying the start-up clock as CCLK, or to supply the appropriate user clock.

Start-up Sequence

The Start-up sequence begins when the configuration memory is full, and the total number of configuration clocks received since $\overline{INIT}$ went High equals the loaded value of the length count.

The next rising clock edge sets a flip-flop Q0, shown in Figure 50. Q0 is the leading bit of a 5-bit shift register. The outputs of this register can be programmed to control three events.

- The release of the open-drain DONE output
- The change of configuration-related pins to the user function, activating all IOBs.
- The termination of the global Set/Reset initialization of all CLB and IOB storage elements.

The DONE pin can also be wire-ANDed with DONE pins of other FPGAs or with other external signals, and can then be used as input to bit Q3 of the start-up register. This is called "Start-up Timing Synchronous to Done In" and is selected by the CCLK_SYNC and UCLK_SYNC MakeBits options.

When DONE is not used as an input, the operation is called "Start-up Timing Not Synchronous to DONE In," and is selected by the CCLK_NOSYNC and UCLK_NOSYNC MakeBits options.

As a configuration option, the start-up control register beyond Q0 can be clocked either by subsequent CCLK pulses or from an on-chip user net called STARTUP.CLK. These signals can be accessed by placing the STARTUP library symbol.

Start-up from CCLK

If CCLK is used to drive the start-up, Q0 through Q3 provide the timing. Heavy lines in Figure 49 show the default timing, which is compatible with XC2000 and XC3000 devices using early DONE and late Reset. The thin lines indicate all other possible timing options.

Start-up from a User Clock (STARTUP.CLK)

When, instead of CCLK, a user-supplied start-up clock is selected, Q1 is used to bridge the unknown phase relationship between CCLK and the user clock. This arbitration causes an unavoidable one-cycle uncertainty in the timing of the rest of the start-up sequence.

DONE Goes High to Signal End of Configuration

In all configuration modes except Express mode, XC4000-Series devices read the expected length count from the bitstream and store it in an internal register. The length count varies according to the number of devices and the composition of the daisy chain. Each device also counts the number of CCLKs during configuration.

Two conditions have to be met in order for the DONE pin to go high:

- the chip's internal memory must be full, and
- the configuration length count must be met, *exactly.*

This is important because the counter that determines when the length count is met begins with the very first CCLK, not the first one after the preamble.

Therefore, if a stray bit is inserted before the preamble, or the data source is not ready at the time of the first CCLK, the internal counter that holds the number of CCLKs will be one ahead of the actual number of data bits read. At the end of configuration, the configuration memory will be full, but the number of bits in the internal counter will not match the expected length count.

As a consequence, a Master mode device will continue to send out CCLKs until the internal counter turns over to zero, and then reaches the correct length count a second time. This will take several seconds [2^{24} * CCLK period] — which is sometimes interpreted as the device not configuring at all.

If it is not possible to have the data ready at the time of the first CCLK, the problem can be avoided by increasing the number in the length count by the appropriate value. The *XACT User Guide* includes detailed information about manually altering the length count.

In Express mode, there is no length count. The DONE pin for each device goes High when the device has received its quota of configuration data. Wiring the DONE pins of several devices together delays start-up of all devices until all are fully configured.

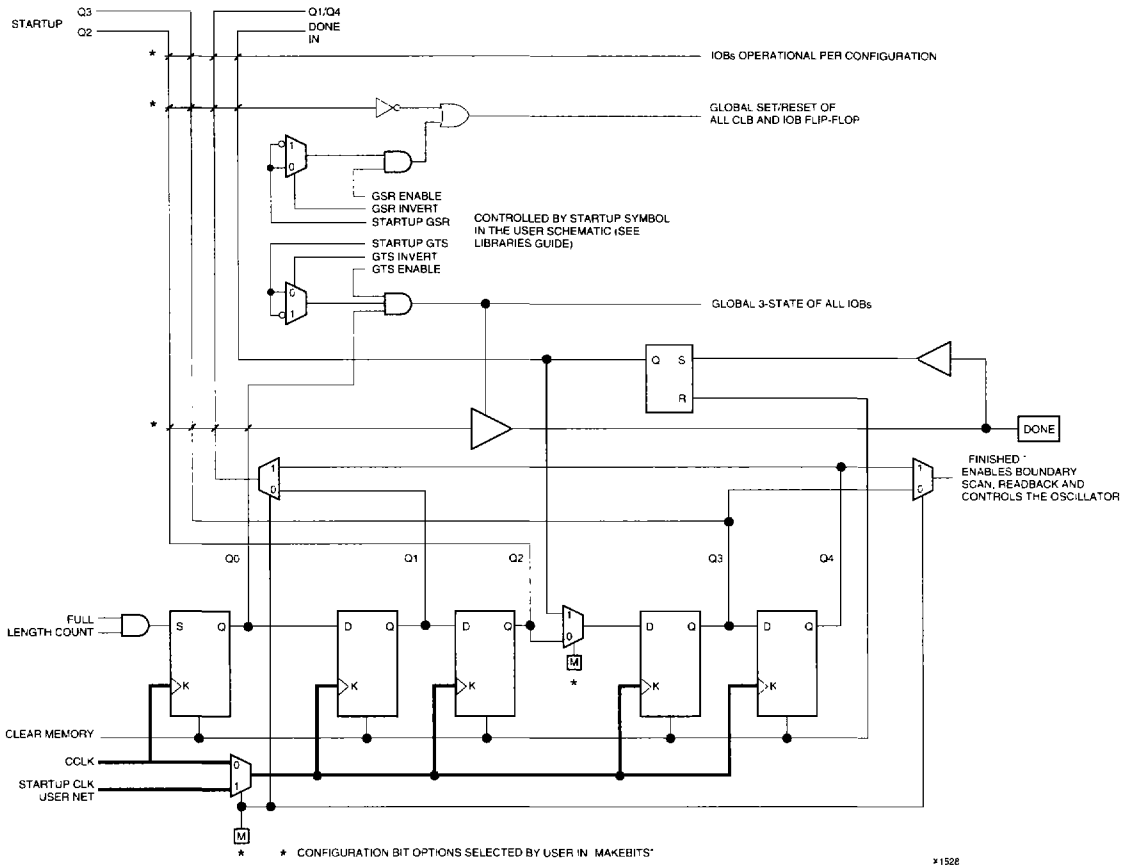


Figure 50: Start-up Logic

Note that DONE is an open-drain output and does not go High unless an internal pull-up is activated or an external pull-up is attached. The internal pull-up is activated as the default by MakeBits, the bitstream generation software.

Release of User I/O After DONE Goes High

By default, the user I/O are released one CCLK cycle after the DONE pin goes High. If CCLK is not clocked after DONE goes High, the outputs remain in their initial state — 3-stated, with a 50 kΩ - 100 kΩ pull-up. The delay from DONE High to active user I/O is controlled by a MakeBits option.

Release of Global Set/Reset After DONE Goes High

By default, Global Set/Reset (GSR) is released two CCLK cycles after the DONE pin goes High. If CCLK is not clocked twice after DONE goes High, all flip-flops are held in their initial set or reset state. The delay from DONE High to GSR inactive is controlled by a MakeBits option.

Configuration Complete After DONE Goes High

Three full CCLK cycles are required after the DONE pin goes High, as shown in Figure 49 on page 61. If CCLK is not clocked three times after DONE goes High, readback cannot be initiated and most boundary scan instructions cannot be used.

Configuration Through the Boundary Scan Pins

XC4000-Series devices can be configured through the boundary scan pins. The basic procedure is as follows:

- Power up the FPGA with $\overline{\text{INIT}}$ held Low (or drive the $\overline{\text{PROGRAM}}$ pin Low for more than 300 ns followed by a High while holding $\overline{\text{INIT}}$ Low). Holding $\overline{\text{INIT}}$ Low allows enough time to issue the CONFIG command to the FPGA. The pin can be used as I/O after configuration if a resistor is used to hold $\overline{\text{INIT}}$ Low.
- Issue the CONFIG command to the TMS input
- Wait for $\overline{\text{INIT}}$ to go High
- Sequence the boundary scan Test Access Port to the SHIFT-DR state
- Toggle TCK to clock data into TDI pin.

The user must account for all TCK clock cycles after INIT goes High, as all of these cycles affect the Length Count compare.

For more detailed information, refer to the Xilinx application note XAPP017, "*Boundary Scan in XC4000 Devices*." This application note also applies to XC4000E and XC4000EX devices.

Readback

The user can read back the content of configuration memory and the level of certain internal nodes without interfering with the normal operation of the device.

Readback not only reports the downloaded configuration bits, but can also include the present state of the device, represented by the content of all flip-flops and latches in CLBs and IOBs, as well as the content of function generators used as RAMs.

Note that in XC4000-Series devices, configuration data is *not* inverted with respect to configuration as it is in XC2000 and XC3000 families.

Readback of Express mode bitstreams results in data that does not resemble the original bitstream, because the bitstream format differs from other modes.

XC4000-Series Readback does not use any dedicated pins, but uses four internal nets (RDBK.TRIG, RDBK.DATA, RDBK.RIP and RDBK.CLK) that can be routed to any IOB. To access the internal Readback signals, place the READBACK library symbol and attach the appropriate pad symbols, as shown in Figure 51.

After Readback has been initiated by a Low-to-High transition on RDBK.TRIG, the RDBK.RIP (Read In Progress) output goes High on the next rising edge of RDBK.CLK. Subsequent rising edges of this clock shift out Readback data on the RDBK.DATA net.

Readback data does not include the preamble, but starts with five dummy bits (all High) followed by the Start bit (Low) of the first frame. The first two data bits of the first frame are always High.

Each frame ends with four error check bits. They are read back as High. The last seven bits of the last frame are also read back as High. An additional Start bit (Low) and an 11-bit Cyclic Redundancy Check (CRC) signature follow, before RDBK.RIP returns Low.

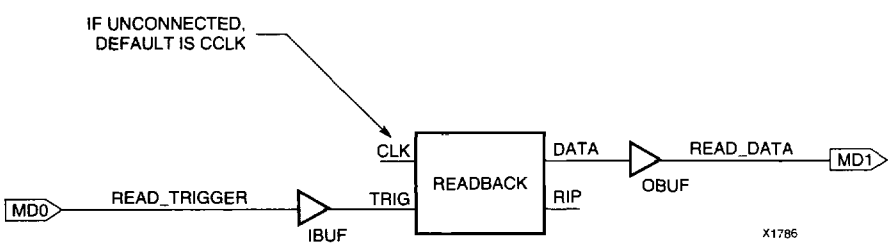


Figure 51: Readback Schematic Example

Readback Options

Readback options are: Read Capture, Read Abort, and Clock Select. They are set with MakeBits, the bitstream generation software.

Read Capture

When the Read Capture option is selected, the readback data stream includes sampled values of CLB and IOB signals. The rising edge of RDBK.TRIG latches the inverted values of the four CLB outputs, the IOB output flip-flops and the input signals I1 and I2. Note that while the bits describing configuration (interconnect, function generators, and RAM content) are *not* inverted, the CLB and IOB output signals *are* inverted.

When the Read Capture option is not selected, the values of the capture bits reflect the configuration data originally written to those memory locations.

If the RAM capability of the CLBs is used, RAM data are available in readback, since they directly overwrite the F and G function-table configuration of the CLB.

RDBK.TRIG is located in the lower-left corner of the device, as shown in Figure 52.

Read Abort

When the Read Abort option is selected, a High-to-Low transition on RDBK.TRIG terminates the readback operation and prepares the logic to accept another trigger.

After an aborted readback, additional clocks (up to one readback clock per configuration frame) may be required to re-initialize the control logic. The status of readback is indicated by the output control net RDBK.RIP. RDBK.RIP is High whenever a readback is in progress.

Clock Select

CCLK is the default clock. However, the user can insert another clock on RDBK.CLK. Readback control and data are clocked on rising edges of RDBK.CLK. If readback must be inhibited for security reasons, the readback control nets are simply not connected.

RDBK.CLK is located in the lower right chip corner, as shown in Figure 52.

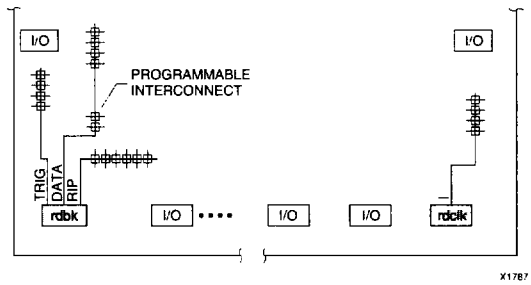


Figure 52: READBACK Symbol in Graphical Editor

Violating the Maximum High and Low Time Specification for the Readback Clock

The readback clock has a maximum High and Low time specification. In some cases, this specification cannot be met. For example, if a processor is controlling readback, an interrupt may force it to stop in the middle of a readback. This necessitates stopping the clock, and thus violating the specification.

The specification is mandatory only on clocking data at the end of a frame prior to the next start bit. The transfer mechanism will load the data to a shift register during the last six clock cycles of the frame, prior to the start bit of the following frame. This loading process is dynamic, and is the source of the maximum High and Low time requirements.

Therefore, the specification only applies to the six clock cycles prior to and including any start bit, including the clocks before the first start bit in the readback data stream. At other times, the frame data is already in the register and the register is not dynamic. Thus, it can be shifted out just like a regular shift register.

The user must precisely calculate the location of the readback data relative to the frame. The system must keep track of the position within a data frame, and disable interrupts before frame boundaries. Frame lengths and data formats are listed in Table 21, Table 22 and Table 23.

Readback with the XChecker Cable

The XChecker Universal Download/Readback Cable and Logic Probe uses the readback feature for bitstream verification. It can also display selected internal signals on the PC or workstation screen, functioning as a low-cost in-circuit emulator.

Configuration Timing

The seven configuration modes are discussed in detail in this section. Timing specifications are included.

Master Serial Mode

In Master Serial mode, the CCLK output of the lead FPGA drives a Xilinx Serial PROM that feeds the FPGA DIN input. Each rising edge of the CCLK output increments the Serial PROM internal address counter. The next data bit is put on the SPROM data output, connected to the FPGA DIN pin. The lead FPGA accepts this data on the subsequent rising CCLK edge.

The lead FPGA then presents the preamble data—and all data that overflows the lead device—on its DOUT pin. There is an internal pipeline delay of 1.5 CCLK periods, which means that DOUT changes on the falling CCLK edge, and the next FPGA in the daisy chain accepts data on the subsequent rising CCLK edge.

In MakeBits, the user can specify Fast ConfigRate, which, starting several bits into the first frame, increases the CCLK frequency by a factor of eight. The value increases from between 0.5 and 1.25 MHz, to a value between 4 and 10 MHz. (For low-voltage devices, the frequency can be up to 10% lower.) Be sure that the serial PROM and slaves are fast enough to support this data rate. XC2000, XC3000/A, and XC3100A devices do not support the Fast ConfigRate option.

The SPROM CE input can be driven from either $\overline{LDC}$ or DONE. Using $\overline{LDC}$ avoids potential contention on the DIN pin, if this pin is configured as user-I/O, but $\overline{LDC}$ is then restricted to be a permanently High user output after configuration. Using DONE can also avoid contention on DIN, provided the early DONE option is invoked.

Master Serial mode is selected by a <000> on the mode pins (M2, M1, M0).

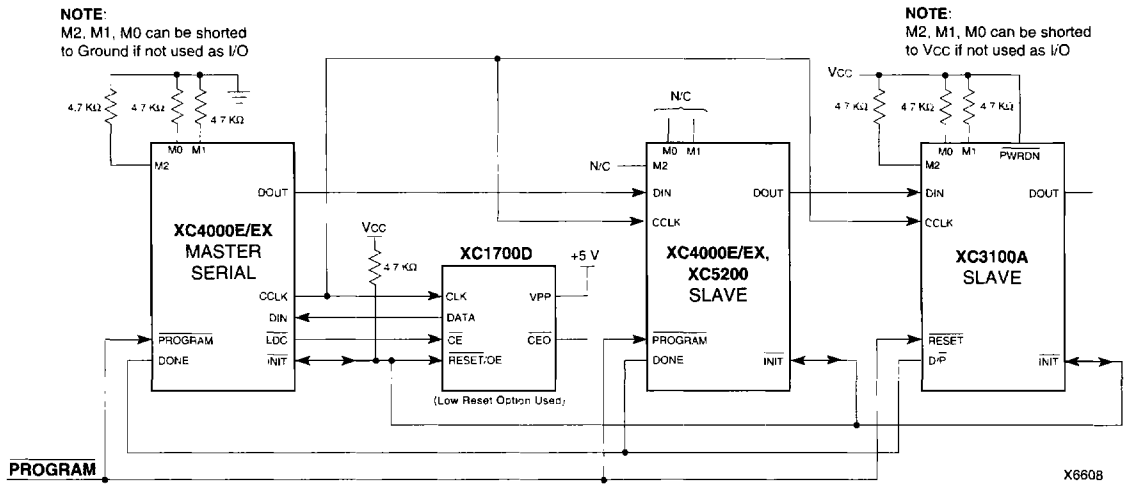
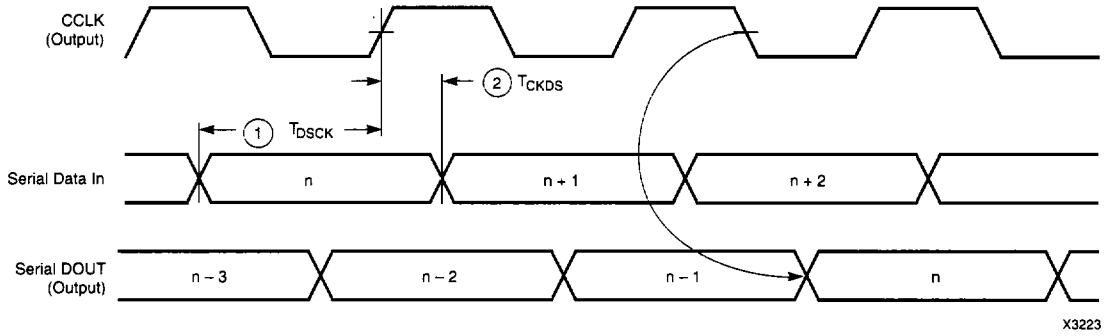


Figure 53: Master Serial Mode Circuit Diagram



	Description		Symbol	Min	Max	Units
CCLK	DIN setup	1	T_{DSCK}	20		ns
	DIN hold	2	T_{CKDS}	0		ns

Notes: 1. At power-up, Vcc must rise from 2.0 V to Vcc min in less than 25 ms, otherwise delay configuration by pulling $\overline{\text{PROGRAM}}$ Low until Vcc is valid.
2. Master Serial mode timing is based on testing in slave mode.

Figure 54: Master Serial Mode Programming Switching Characteristics

Slave Serial Mode

In Slave Serial mode, an external signal drives the CCLK input of the FPGA. The serial configuration bitstream must be available at the DIN input of the lead FPGA a short setup time before each rising CCLK edge.

The lead FPGA then presents the preamble data—and all data that overflows the lead device—on its DOUT pin. There is an internal delay of 0.5 CCLK periods, which means that DOUT changes on the falling CCLK edge, and the next FPGA in the daisy chain accepts data on the subsequent rising CCLK edge.

Slave Serial mode is selected by a <111> on the mode pins (M2, M1, M0). Slave Serial is the default mode if the mode pins are left unconnected, as they have weak pull-up resistors during configuration.

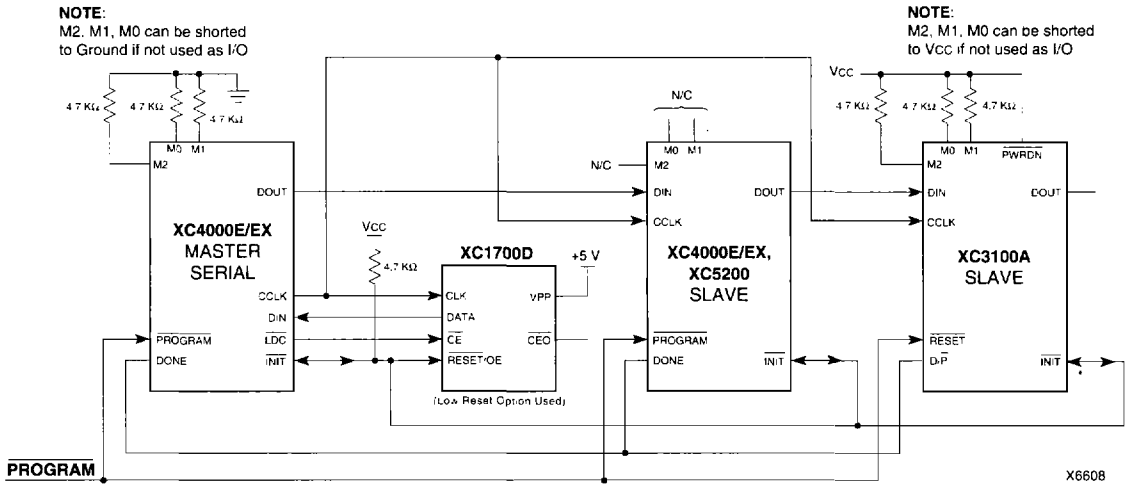
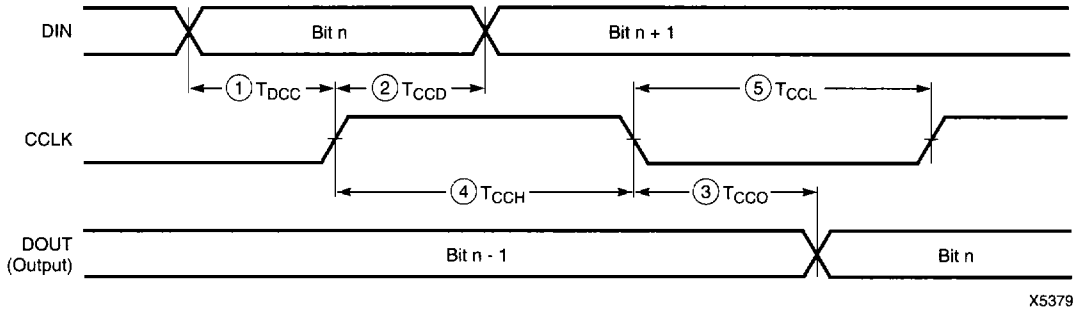


Figure 55: Slave Serial Mode Circuit Diagram



	Description		Symbol	Min	Max	Units
CCLK	DIN setup	1	T_{DCC}	20		ns
	DIN hold	2	T_{CCD}	0		ns
	DIN to DOUT	3	T_{CCO}		30	ns
	High time	4	T_{CCH}	45		ns
	Low time	5	T_{CCL}	45		ns
	Frequency		F_{CC}		10	MHz

Note: Configuration must be delayed until the $\overline{INIT}$ pins of all daisy-chained FPGAs are High.

Figure 56: Slave Serial Mode Programming Switching Characteristics

Master Parallel Modes

In the two Master Parallel modes, the lead FPGA directly addresses an industry-standard byte-wide EPROM, and accepts eight data bits just before incrementing or decrementing the address outputs.

The eight data bits are serialized in the lead FPGA, which then presents the preamble data—and all data that overflows the lead device—on its DOUT pin. There is an internal delay of 1.5 CCLK periods, after the rising CCLK edge that accepts a byte of data (and also changes the EPROM address) until the falling CCLK edge that makes the LSB (D0) of this byte appear at DOUT. This means that DOUT changes on the falling CCLK edge, and the next FPGA in the daisy chain accepts data on the subsequent rising CCLK edge.

The PROM address pins can be incremented or decremented, depending on the mode pin settings. This option allows the FPGA to share the PROM with a wide variety of microprocessors and microcontrollers. Some processors must boot from the bottom of memory (all zeros) while others must boot from the top. The FPGA is flexible and can load its configuration bitstream from either end of the memory.

Master Parallel Up mode is selected by a <100> on the mode pins (M2, M1, M0). The EPROM addresses start at 00000 and increment.

Master Parallel Down mode is selected by a <110> on the mode pins. The EPROM addresses start at 3FFFF and decrement.

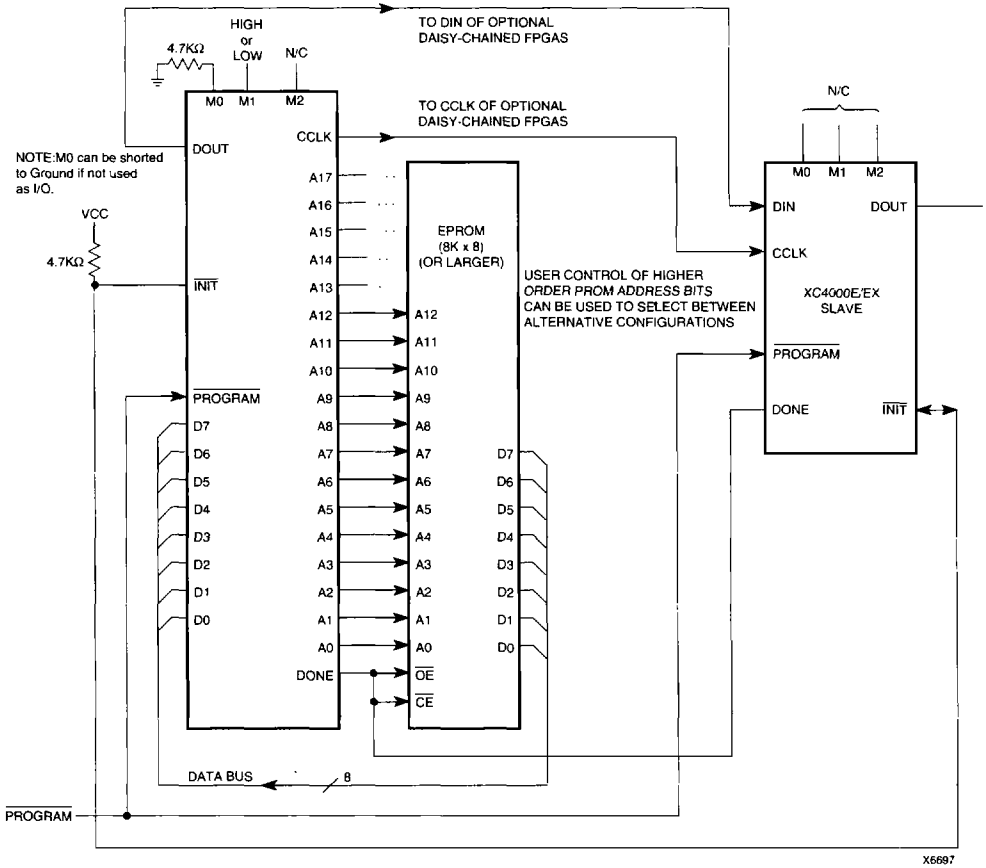
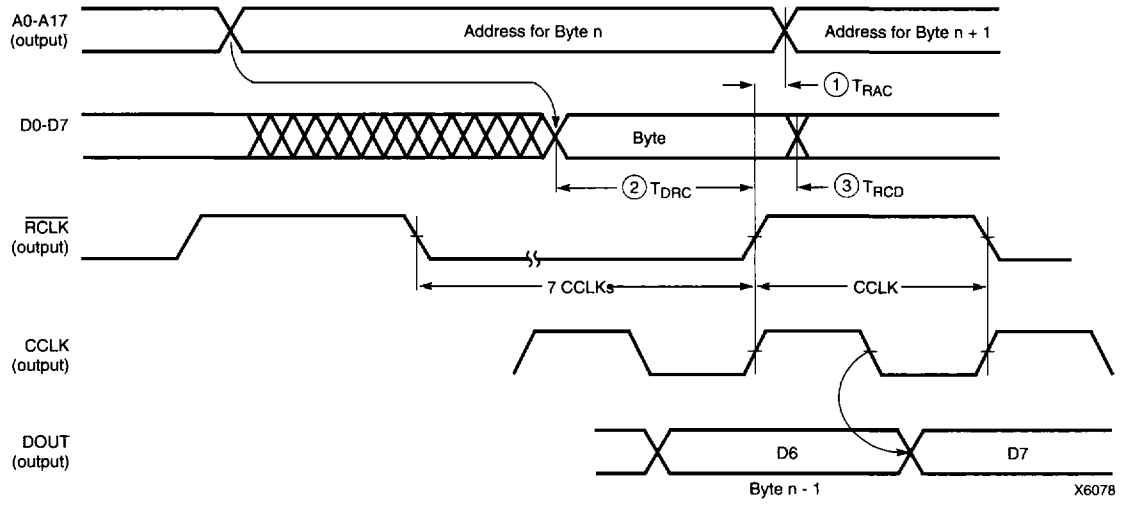


Figure 57: Master Parallel Mode Circuit Diagram



	Description	Symbol		Min	Max	Units
RCLK	Delay to Address valid	1	T_{RAC}	0	200	ns
	Data setup time	2	T_{DRC}	60		ns
	Data hold time	3	T_{RCD}	0		ns

Notes: 1. At power-up, Vcc must rise from 2.0 V to Vcc min in less than 25 ms, otherwise delay configuration by pulling $\overline{\text{PROGRAM}}$ Low until Vcc is valid.
2. The first Data byte is loaded and CCLK starts at the end of the first $\overline{\text{RCLK}}$ active cycle (rising edge).

This timing diagram shows that the EPROM requirements are extremely relaxed. EPROM access time can be longer than 500 ns. EPROM data output has no hold-time requirements.

Figure 58: Master Parallel Mode Programming Switching Characteristics

Synchronous Peripheral Mode

Synchronous Peripheral mode can also be considered Slave Parallel mode. An external signal drives the CCLK input(s) of the FPGA(s). The first byte of parallel configuration data must be available at the Data inputs of the lead FPGA a short setup time before the rising CCLK edge. Subsequent data bytes are clocked in on every eighth consecutive rising CCLK edge.

The same CCLK edge that accepts data, also causes the RDY/$\overline{\text{BUSY}}$ output to go High for one CCLK period. The pin name is a misnomer. In Synchronous Peripheral mode it is really an ACKNOWLEDGE signal. Synchronous operation does not require this response, but it is a meaningful signal for test purposes. Note that RDY/$\overline{\text{BUSY}}$ is pulled High with a high-impedance pullup prior to $\overline{\text{INIT}}$ going High.

The lead FPGA serializes the data and presents the preamble data (and all data that overflows the lead device) on its DOUT pin. There is an internal delay of 1.5 CCLK periods, which means that DOUT changes on the falling CCLK edge, and the next FPGA in the daisy chain accepts data on the subsequent rising CCLK edge.

In order to complete the serial shift operation, 10 additional CCLK rising edges are required after the last data byte has been loaded, plus one more CCLK cycle for each daisy-chained device.

Synchronous Peripheral mode is selected by a <011> on the mode pins (M2, M1, M0).

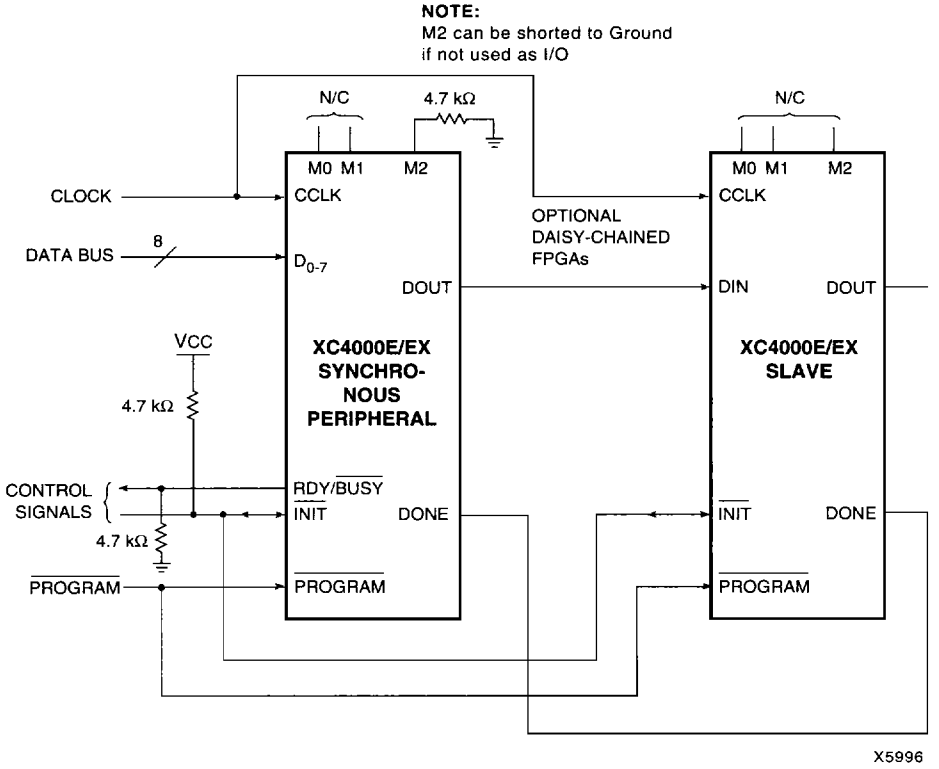
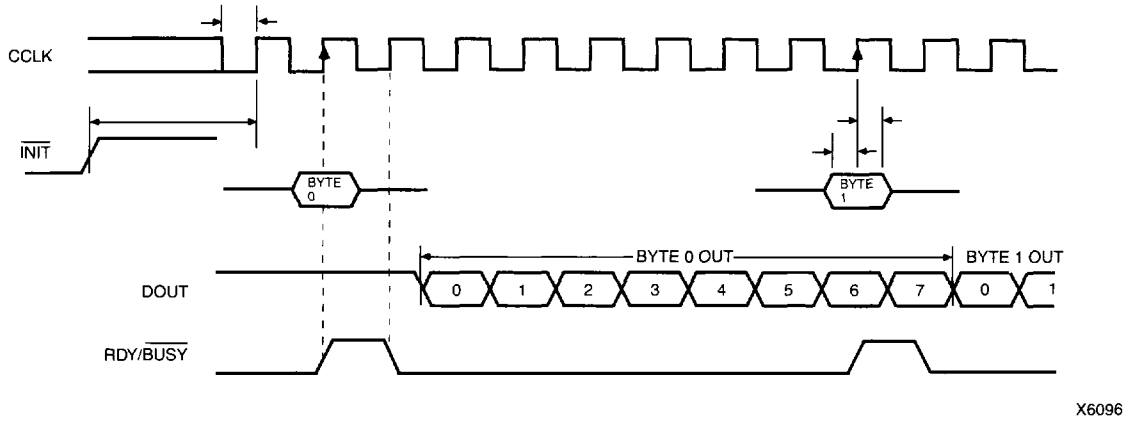


Figure 59: Synchronous Peripheral Mode Circuit Diagram



	Description	Symbol	Min	Max	Units
CCLK	INIT (High) setup time	T_{IC}	5		µs
	D0 - D7 setup time	T_{DC}	60		ns
	D0 - D7 hold time	T_{CD}	0		ns
	CCLK High time	T_{CCH}	50		ns
	CCLK Low time	T_{CCL}	60		ns
	CCLK Frequency	F_{CC}		8	MHz

Notes:
1. Peripheral Synchronous mode can be considered Slave Parallel mode. An external CCLK provides timing. clocking in the **first** data byte on the **second** rising edge of CCLK after INIT goes High. Subsequent data bytes are clocked in on every eighth consecutive rising edge of CCLK.
2. The RDY/BUSY line goes High for one CCLK period after data has been clocked in, although synchronous operation does not require such a response.
3. The pin name RDY/BUSY is a misnomer. In Synchronous Peripheral mode this is really an ACKNOWLEDGE signal.
4. Note that data starts to shift out serially on the DOUT pin 0.5 CCLK periods after it was loaded in parallel. Therefore, additional CCLK pulses are clearly required after the last byte has been loaded.

Figure 60: Synchronous Peripheral Mode Programming Switching Characteristics

Asynchronous Peripheral Mode

Write to FPGA

Asynchronous Peripheral mode uses the trailing edge of the logic AND condition of $\overline{WS}$ and $\overline{CS0}$ being Low and $\overline{RS}$ and CS1 being High to accept byte-wide data from a microprocessor bus. In the lead FPGA, this data is loaded into a double-buffered UART-like parallel-to-serial converter and is serially shifted into the internal logic.

The lead FPGA presents the preamble data (and all data that overflows the lead device) on its DOUT pin. The RDY/$\overline{BUSY}$ output from the lead FPGA acts as a handshake signal to the microprocessor. RDY/$\overline{BUSY}$ goes Low when a byte has been received, and goes High again when the byte-wide input buffer has transferred its information into the shift register, and the buffer is ready to receive new data. A new write may be started immediately, as soon as the RDY/$\overline{BUSY}$ output has gone Low, acknowledging receipt of the previous data. Write may not be terminated until RDY/$\overline{BUSY}$ is High again for one CCLK period. Note that RDY/$\overline{BUSY}$ is pulled High with a high-impedance pull-up prior to $\overline{INIT}$ going High.

The length of the $\overline{BUSY}$ signal depends on the activity in the UART. If the shift register was empty when the new byte was received, the $\overline{BUSY}$ signal lasts for only two CCLK periods. If the shift register was still full when the new byte was received, the $\overline{BUSY}$ signal can be as long as nine CCLK periods.

Note that after the last byte has been entered, only seven of its bits are shifted out. CCLK remains High with DOUT equal to bit 6 (the next-to-last bit) of the last byte entered.

The READY/$\overline{BUSY}$ handshake can be ignored if the delay from any one Write to the end of the next Write is guaranteed to be longer than 10 CCLK periods.

Status Read

The logic AND condition of the $\overline{CS0}$, CS1and $\overline{RS}$ inputs puts the device status on the Data bus.

- D7 High indicates Ready
- D7 Low indicates Busy
- D0 through D6 go unconditionally High

It is mandatory that the whole start-up sequence be started and completed by one byte-wide input. Otherwise, the pins used as Write Strobe or Chip Enable might become active outputs and interfere with the final byte transfer. If this transfer does not occur, the start-up sequence is not completed all the way to the finish (point F in Figure 49 on page 61).

In this case, at worst, the internal reset is not released. At best, Readback and Boundary Scan are inhibited. The length-count value, as generated by MakeBits and MakePROM, ensures that these problems never occur.

Although RDY/$\overline{BUSY}$ is brought out as a separate signal, microprocessors can more easily read this information on one of the data lines. For this purpose, D7 represents the RDY/$\overline{BUSY}$ status when $\overline{RS}$ is Low, $\overline{WS}$ is High, and the two chip select lines are both active.

Asynchronous Peripheral mode is selected by a <101> on the mode pins (M2, M1, M0).

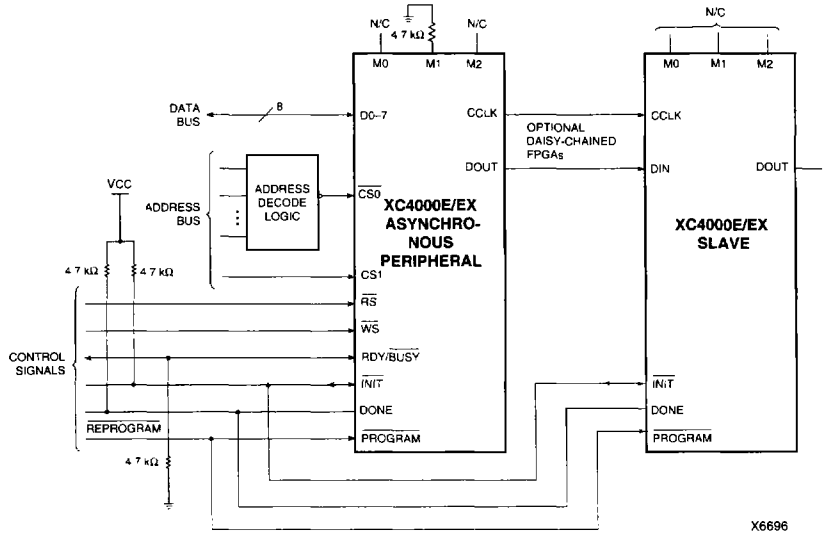
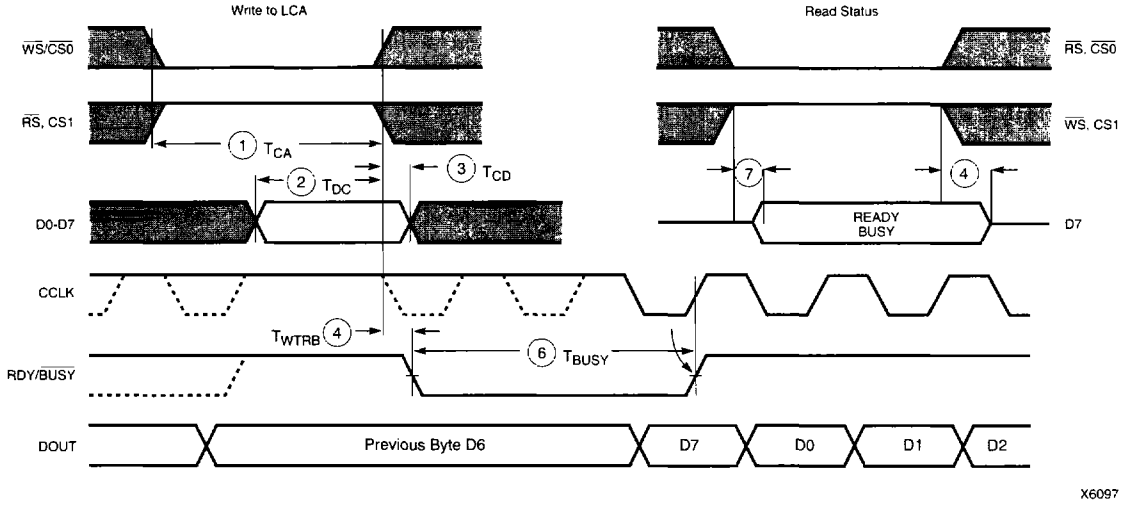


Figure 61: Asynchronous Peripheral Mode Circuit Diagram



	Description		Symbol	Min	Max	Units
Write	Effective Write time ($\overline{CS0}$, $\overline{WS}$=Low; $\overline{RS}$, CS1=High)	1	T_{CA}	100		ns
	DIN setup time	2	T_{DC}	60		ns
	DIN hold time	3	T_{CD}	0		ns
RDY	$\overline{RDY/BUSY}$ delay after end of Write or Read	4	T_{WTRB}		60	ns
	$\overline{RDY/BUSY}$ active after beginning of Read	7			60	ns
	$\overline{RDY/BUSY}$ Low output (Note 4)	6	T_{BUSY}	2	9	CCLK periods

Notes:
1. Configuration must be delayed until the $\overline{INIT}$ pins of all daisy-chained FPGAs are High.
2. The time from the end of $\overline{WS}$ to CCLK cycle for the new byte of data depends on the completion of previous byte processing and the phase of the internal timing generator for CCLK.
3. *CCLK and DOUT timing is tested in slave mode.*
4. T_{BUSY} indicates that the double-buffered parallel-to-serial converter is not yet ready to receive new data. The shortest T_{BUSY} occurs when a byte is loaded into an empty parallel-to-serial converter. The longest T_{BUSY} occurs when a new word is loaded into the input register before the second-level buffer has started shifting out data.

This timing diagram shows very relaxed requirements. Data need not be held beyond the rising edge of $\overline{WS}$. $\overline{RDY/BUSY}$ will go active within 60 ns after the end of $\overline{WS}$. A new write may be asserted immediately after $\overline{RDY/BUSY}$ goes Low, but write may not be terminated until $\overline{RDY/BUSY}$ has been High for one CCLK period.

Figure 62: Asynchronous Peripheral Mode Programming Switching Characteristics

Express Mode (XC4000EX only)

Express mode is similar to Slave Serial mode, except that data is processed one byte per CCLK cycle instead of one bit per CCLK cycle. An external source is used to drive CCLK, while byte-wide data is loaded directly into the configuration data shift registers. A CCLK frequency of 1 MHz is equivalent to a 8 MHz serial rate, because eight bits of configuration data are loaded per CCLK cycle. Express mode does not support CRC error checking, but does support constant-field error checking.

In Express mode, an external signal drives the CCLK input of the FPGA device. The first byte of parallel configuration data must be available at the D inputs of the FPGA a short setup time before the second rising CCLK edge. Subsequent data bytes are clocked in on each consecutive rising CCLK edge.

Express mode is only supported by the XC4000EX and XC5200 families. It may not be used, therefore, when an XC4000EX or XC5200 device is daisy-chained with devices from other Xilinx families.

If the first device is configured in Express mode, additional devices may be daisy-chained only if every device in the chain is also configured in Express mode. CCLK pins are tied together and D0-D7 pins are tied together for all devices along the chain. A status signal is passed from DOUT to CS1 of successive devices along the chain. The lead device in the chain has its CS1 input tied High (or floating, since there is an internal pullup). Frame data is accepted only when CS1 is High and the device's configuration memory is not already full. The status pin DOUT is pulled Low two internal-oscillator cycles after $\overline{INIT}$ is recognized as High, and remains Low until the device's configuration memory is full. DOUT is then pulled High to signal the next device in the chain to accept the configuration data on the D0-D7 bus.

The DONE pins of all devices in the chain should be tied together, with one or more active internal pull-ups. If a large number of devices are included in the chain, deactivate some of the internal pull-ups, since the Low-driving DONE pin of the last device in the chain must sink the current from all pull-ups in the chain. The DONE pull-up is activated by default. It can be deactivated using a MakeBits option.

XC4000EX devices in Express mode are always synchronized to DONE. The device becomes active after DONE goes High. DONE is an open-drain output. With the DONE pins tied together, therefore, the external DONE signal stays low until all devices are configured, then all devices in the daisy chain become active simultaneously. If the DONE pin of a device is left unconnected, the device becomes active as soon as that device has been configured. XC5200 devices in the chain should be configured as synchronized to DONE (MakeBits option CCLK_SYNC or UCLK_SYNC), and their DONE pins wired together with those of the XC4000EX devices.

Express mode must be specified as an option to the MakeBits program, which generates the bitstream. The Express mode bitstream is not compatible with the other six configuration modes.

Express mode is selected by a <010> on the mode pins (M2, M1, M0).

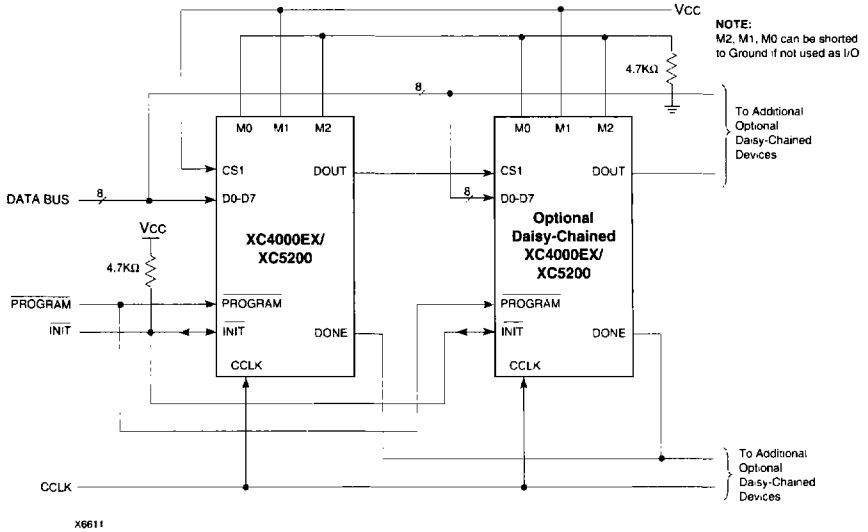
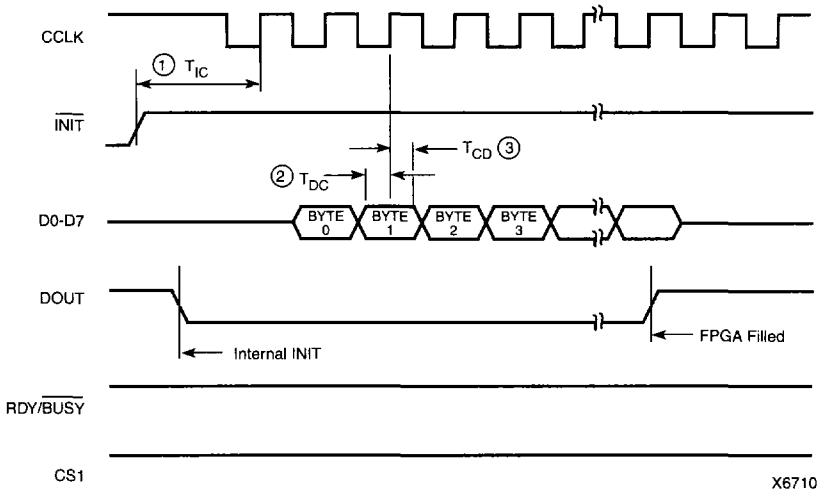


Figure 63: Express Mode Circuit Diagram

	Description	Symbol	Min	Max	Units
CCLK	$\overline{INIT}$ (High) setup time	T_{IC}	-		µs
	D0 - D7 setup time	T_{DC}	-		ns
	D0 - D7 hold time	T_{CD}	0		ns
	CCLK High time	T_{CCH}	-		ns
	CCLK Low time	T_{CCL}	-		ns
	CCLK Frequency	F_{CC}		-	MHz
			Preliminary		



Note: If not driven by the preceding DOUT. CS1 *must* remain High until the device is fully configured.

Figure 64: Express Mode Programming Switching Characteristics

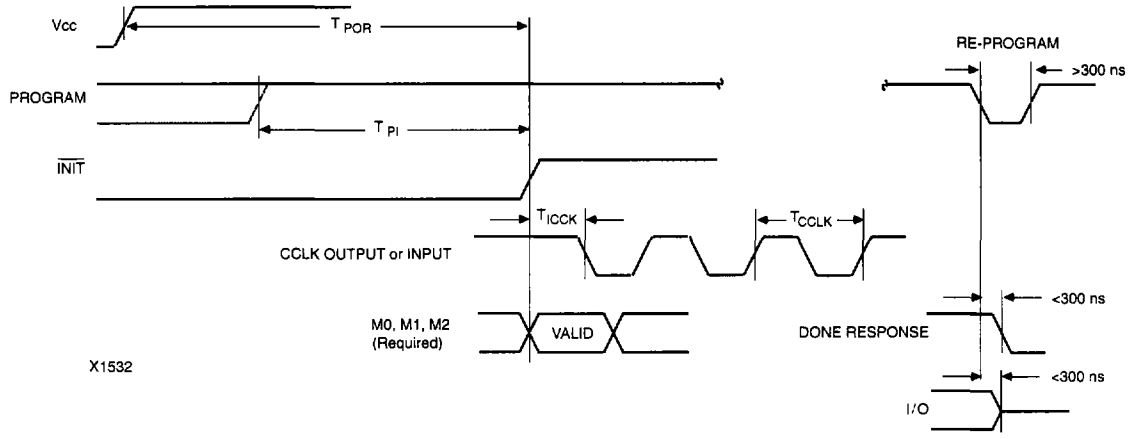
Table 24: Pin Functions During Configuration

CONFIGURATION MODE <M2:M1:M0>							
SLAVE SERIAL <1:1:1>	MASTER SERIAL <0:0:0>	SYNCH. PERIPHERAL <0:1:1>	ASYNCH. PERIPHERAL <1:0:1>	MASTER PARALLEL DOWN <1:1:0>	MASTER PARALLEL UP <1:0:0>	EXPRESS <0:1:0>	USER OPERATION
M2(HIGH) (I)	M2(LOW) (I)	M2(LOW) (I)	M2(HIGH) (I)	M2(HIGH) (I)	M2(HIGH) (I)	M2(LOW) (I)	(I)
M1(HIGH) (I)	M1(LOW) (I)	M1(HIGH) (I)	M1(LOW) (I)	M1(HIGH) (I)	M1(LOW) (I)	M1(HIGH) (I)	(O)
M0(HIGH) (I)	M0(LOW) (I)	M0(HIGH) (I)	M0(HIGH) (I)	M0(LOW) (I)	M0(LOW) (I)	M0(HIGH) (I)	(I)
HDC (HIGH)	HDC (HIGH)	HDC (HIGH)	HDC (HIGH)	HDC (HIGH)	HDC (HIGH)	HDC (HIGH)	I/O
$\overline{\text{LDC}}$ (LOW)	$\overline{\text{LDC}}$ (LOW)	$\overline{\text{LDC}}$ (LOW)	$\overline{\text{LDC}}$ (LOW)	$\overline{\text{LDC}}$ (LOW)	$\overline{\text{LDC}}$ (LOW)	$\overline{\text{LDC}}$ (LOW)	I/O
$\overline{\text{INIT}}$	$\overline{\text{INIT}}$	$\overline{\text{INIT}}$	$\overline{\text{INIT}}$	$\overline{\text{INIT}}$	$\overline{\text{INIT}}$	$\overline{\text{INIT}}$	I/O
DONE	DONE	DONE	DONE	DONE	DONE	DONE	DONE
PROGRAM (I)	PROGRAM (I)	PROGRAM (I)	PROGRAM (I)	PROGRAM (I)	PROGRAM (I)	PROGRAM (I)	PROGRAM
CCLK (I)	CCLK (O)	CCLK (I)	CCLK (O)	CCLK (O)	CCLK (O)	CCLK (I)	CCLK (I)
		RDY/$\overline{\text{BUSY}}$ (O)	RDY/$\overline{\text{BUSY}}$ (O)	$\overline{\text{RCLK}}$ (O)	$\overline{\text{RCLK}}$ (O)		I/O
			$\overline{\text{RS}}$ (I)				I/O
			$\overline{\text{CS0}}$ (I)				I/O
		DATA 7 (I)	DATA 7 (I)	DATA 7 (I)	DATA 7 (I)	DATA 7 (I)	I/O
		DATA 6 (I)	DATA 6 (I)	DATA 6 (I)	DATA 6 (I)	DATA 6 (I)	I/O
		DATA 5 (I)	DATA 5 (I)	DATA 5 (I)	DATA 5 (I)	DATA 5 (I)	I/O
		DATA 4 (I)	DATA 4 (I)	DATA 4 (I)	DATA 4 (I)	DATA 4 (I)	I/O
		DATA 3 (I)	DATA 3 (I)	DATA 3 (I)	DATA 3 (I)	DATA 3 (I)	I/O
		DATA 2 (I)	DATA 2 (I)	DATA 2 (I)	DATA 2 (I)	DATA 2 (I)	I/O
		DATA 1 (I)	DATA 1 (I)	DATA 1 (I)	DATA 1 (I)	DATA 1 (I)	I/O
DIN (I)	DIN (I)	DATA 0 (I)	DATA 0 (I)	DATA 0 (I)	DATA 0 (I)	DATA 0 (I)	I/O
DOUT	DOUT	DOUT	DOUT	DOUT	DOUT	DOUT	SGCK4-GCK5-I/O
TDI	TDI	TDI	TDI	TDI	TDI	TDI	TDI-I/O
TCK	TCK	TCK	TCK	TCK	TCK	TCK	TCK-I/O
TMS	TMS	TMS	TMS	TMS	TMS	TMS	TMS-I/O
TDO	TDO	TDO	TDO	TDO	TDO	TDO	TDO-(O)
			$\overline{\text{WS}}$ (I)	A0	A0		I/O
				A1	A1		PGCK4-GCK6-I/O
			CS1	A2	A2		I/O
				A3	A3		I/O
				A4	A4		I/O
				A5	A5		I/O
				A6	A6		I/O
				A7	A7		I/O
				A8	A8		I/O
				A9	A9		I/O
				A10	A10		I/O
				A11	A11		I/O
				A12	A12		I/O
				A13	A13		I/O
				A14	A14		I/O
				A15	A15		SGCK1-GCK7-I/O
				A16	A16		PGCK1-GCK8-I/O
				A17	A17		I/O
				A18*	A18*		I/O
				A19*	A19*		I/O
				A20*	A20*		I/O
				A21*	A21*		I/O
							ALL OTHERS

* XC4000EX only

Notes 1. A shaded table cell represents a 50 kΩ - 100 kΩ pull-up before and during configuration.
2. (I) represents an input; (O) represents an output.
3. $\overline{\text{INIT}}$ is an open-drain output during configuration.

Configuration Switching Characteristics



Master Modes

Description		Symbol	Min	Max	Units
Power-On Reset	M0 = High	T_{POR}	10	40	ms
	M0 = Low	T_{POR}	40	130	ms
Program Latency		T_{PI}	30	200	µs per CLB column
CCLK (output) Delay		T_{ICCK}	40	250	µs
CCLK (output) Period, slow		T_{CCLK}	640	2000	ns
CCLK (output) Period, fast		T_{CCLK}	80	250	ns

Slave and Peripheral Modes

Description	Symbol	Min	Max	Units
Power-On Reset	T_{POR}	10	33	ms
Program Latency	T_{PI}	30	200	µs per CLB column
CCLK (input) Delay (required)	T_{ICCK}	4		µs
CCLK (input) Period (required)	T_{CCLK}	100		ns

XC4000E Switching Characteristics

Definition of Terms

In the following tables, some specifications may be designated as Advance or Preliminary. These terms are defined as follows:

Advance: Initial estimates based on simulation and/or extrapolation from other speed grades, devices, or device families. Use as estimates, not for production.
Preliminary: Based on preliminary characterization. Further changes are not expected.
Unmarked: Specifications not identified as either Advance or Preliminary are to be considered Final.[1]

XC4000E Operating Conditions

Symbol	Description		Min	Max	Units
V_{CC}	Supply voltage relative to GND, T_J = -0 °C to +85°C	Commercial	4.75	5.25	V
	Supply voltage relative to GND, T_J = -40°C to +100°C	Industrial	4.5	5.5	V
	Supply voltage relative to GND, T_C = -55°C to +125°C	Military	4.5	5.5	V
V_{IH}	High-level input voltage	TTL inputs	2.0	V_{CC}	V
		CMOS inputs	70%	100%	V_{CC}
V_{IL}	Low-level input voltage	TTL inputs	0	0.8	V
		CMOS inputs	0	20%	V_{CC}
T_{IN}	Input signal transition time (Note 2)			250	ns

Note 1: At junction temperatures above those listed as Operating Conditions, all delay parameters increase by 0.35% per °C.
Note 2: Typical value only. Not tested or characterized.

XC4000E DC Characteristics Over Operating Conditions

Symbol	Description		Min	Max	Units
V_{OH}	High-level output voltage @ I_{OH} = -4.0mA, V_{CC} min	TTL outputs	2.4		V
	High-level output voltage @ I_{OH} = -1.0mA, V_{CC} min	CMOS outputs	V_{CC}-0.5		V
V_{OL}	Low-level output voltage @ I_{OL} = 12.0mA, V_{CC} min (Note 1)	TTL outputs		0.4	V
		CMOS outputs		0.4	V
I_{CCO}	Quiescent FPGA supply current (Note 2)	TTL input levels		10	mA
		CMOS input levels		1	mA
I_L	Input or output leakage current		-10	+10	µA
C_{IN}	Input capacitance (sample tested)	PQFP and MQFP packages		10	pF
		Other packages		16	pF
I_{RIN}	Pad pull-up (when selected) @ V_{IN} = 0V (sample tested)		0.02	0.25	mA
I_{RLL}	Horizontal Longline pull-up (when selected) @ logic Low		0.2	2.5	mA

Note 1: With 50% of the outputs simultaneously sinking 12mA, up to a maximum of 64 pins.
Note 2: With no output current loads, no active input or Longline pull-up resistors, all package pins at Vcc or GND, and the FPGA configured with a MakeBits Tie option.

1. Notwithstanding the definition of the above terms, all specifications are subject to change without notice.

XC4000E Absolute Maximum Ratings

Symbol	Description			Units
V_{CC}	Supply voltage relative to GND		-0.5 to +7.0	V
V_{IN}	Input voltage relative to GND (Note 1)		-0.5 to V_{CC} +0.5	V
V_{TS}	Voltage applied to 3-state output (Note 1)		-0.5 to V_{CC} +0.5	V
T_{STG}	Storage temperature (ambient)		-65 to +150	°C
T_{SOL}	Maximum soldering temperature (10 s @ 1/16 in. = 1.5 mm)		+260	°C
T_J	Junction temperature	Ceramic packages	+150	°C
		Plastic packages	+125	°C

Note 1: Maximum DC overshoot or undershoot above Vcc or below GND must be limited to either 0.5 V or 10 mA, whichever is easier to achieve. During transitions, the device pins may undershoot to -2.0 V or overshoot to Vcc + 2.0 V, provided this over- or undershoot lasts less than 20 ns.

Note 2: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

XC4000E Global Buffer Switching Characteristic Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are not measured directly. They are derived from benchmark timing patterns that are taken at device introduction, prior to any process improvements. For more detailed, more precise, and more up-to-date information, use the values provided by the XACT timing calculator and used in the simulator. These values can be printed in tabular format by running LCA2XNF -S.

The following guidelines reflect worst-case values over the recommended operating conditions.

		Speed Grade	-4	-3	-2		
Description	**Symbol**	**Device**	**Max**	**Max**	**Max**		**Units**
From pad through Primary buffer, to any clock K	T_{PG}	XC4003E	7.0	4.7	4.0		ns
		XC4005E	7.0	4.7	4.0		ns
		XC4006E	7.5	5.3	4.5		ns
		XC4008E	8.0	6.1	5.2		ns
		XC4010E	11.0	6.3	5.4		ns
		XC4013E	11.5	6.8	5.8		ns
		XC4020E	12.0	7.0	6.2		ns
		XC4025E	12.5	7.2	6.3		ns
From pad through Secondary buffer, to any clock K	T_{SG}	XC4003E	7.5	5.2	4.4		ns
		XC4005E	7.5	5.2	4.4		ns
		XC4006E	8.0	5.8	4.9		ns
		XC4008E	8.5	6.6	5.6		ns
		XC4010E	11.5	6.8	5.8		ns
		XC4013E	12.0	7.3	6.2		ns
		XC4020E	12.5	7.5	6.6		ns
		XC4025E	13.0	7.7	6.8		ns
			PRELIMINARY		ADVANCE		

XC4000E Wide Decoder Switching Characteristic Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are not measured directly. They are derived from benchmark timing patterns that are taken at device introduction, prior to any process improvements. For more detailed, more precise, and more up-to-date information, use the values provided by the XACT timing calculator and used in the simulator. These values can be printed in tabular format by running LCA2XNF -S.

The following guidelines reflect worst-case values over the recommended operating conditions.

		Speed Grade	-4	-3	-2	
Description	**Symbol**	**Device**	**Max**	**Max**	**Max**	**Units**
Full length, both pull-ups, inputs from IOB I-pins	T_{WAF}	XC4003E	9.2	5.0	4.3	ns
		XC4005E	9.5	6.0	5.1	ns
		XC4006E	12.0	7.0	6.2	ns
		XC4008E	12.5	8.0	7.0	ns
		XC4010E	15.0	9.0	8.1	ns
		XC4013E	16.0	11.0	9.9	ns
		XC4020E	17.0	13.9	12.5	ns
		XC4025E	18.0	16.9	15.2	ns
Full length, both pull-ups, inputs from internal logic	T_{WAFL}	XC4003E	12.0	7.0	6.0	ns
		XC4005E	12.5	8.0	6.8	ns
		XC4006E	14.0	9.0	7.9	ns
		XC4008E	16.0	10.0	8.8	ns
		XC4010E	18.0	11.0	9.7	ns
		XC4013E	19.0	13.0	11.7	ns
		XC4020E	20.0	15.5	14.0	ns
		XC4025E	21.0	18.9	17.0	ns
Half length, one pull-up, inputs from IOB I-pins	T_{WAO}	XC4003E	10.5	6.0	5.1	ns
		XC4005E	10.5	7.0	6.0	ns
		XC4006E	13.5	8.0	6.8	ns
		XC4008E	14.0	9.0	7.9	ns
		XC4010E	16.0	10.0	8.8	ns
		XC4013E	17.0	12.0	10.8	ns
		XC4020E	18.0	15.0	13.5	ns
		XC4025E	19.0	17.6	15.8	ns
Half length, one pull-up, inputs from internal logic	T_{WAOL}	XC4003E	12.0	8.0	6.8	ns
		XC4005E	12.5	9.0	7.7	ns
		XC4006E	14.0	10.0	8.5	ns
		XC4008E	16.0	11.0	9.4	ns
		XC4010E	18.0	12.0	10.2	ns
		XC4013E	19.0	14.0	11.9	ns
		XC4020E	20.0	16.8	14.3	ns
		XC4025E	21.0	19.6	16.7	ns
			PRELIMINARY		ADVANCE	

Note 1: These values include a minimum load. The values reported by LCA2XNF -S include only a portion of this delay, therefore the values cannot be directly compared. Use XDelay to determine the delay for each destination.

Note 2: These delays are specified from the decoder input to the decoder output. For pin-to-pin delays, add the input delay (T_{PID}) and output delay (T_{OPF} or T_{OPS}), as listed under "IOB Switching Characteristic Guidelines."

XC4000E Horizontal Longline Switching Characteristic Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are not measured directly. They are derived from benchmark timing patterns that are taken at device introduction, prior to any process improvements. For more detailed, more precise, and more up-to-date information, use the values provided by the XACT timing calculator and used in the simulator. These values can be printed in tabular format by running LCA2XNF -S.

The following guidelines reflect worst-case values over the recommended operating conditions.

		Speed Grade	-4	-3	-2	
Description	**Symbol**	**Device**	**Max**	**Max**	**Max**	**Units**
TBUF driving a Horizontal Longline (LL): I going High or Low to LL going High or Low, while T is Low. Buffer is constantly active. (Note1)	T_{IO1}	XC4003E	5.0	4.2	3.4	ns
		XC4005E	5.0	5.0	4.0	ns
		XC4006E	6.0	5.9	4.7	ns
		XC4008E	7.0	6.3	5.0	ns
		XC4010E	8.0	6.4	5.1	ns
		XC4013E	9.0	7.2	5.7	ns
		XC4020E	10.0	8.2	6.6	ns
		XC4025E	11.0	9.1	7.3	ns
I going Low to LL going from resistive pull-up High to active Low. TBUF configured as open-drain. (Note1)	T_{IO2}	XC4003E	5.0	4.2	3.6	ns
		XC4005E	6.0	5.3	4.5	ns
		XC4006E	7.8	6.4	5.4	ns
		XC4008E	8.1	6.8	5.8	ns
		XC4010E	10.5	6.9	5.9	ns
		XC4013E	11.0	7.7	6.5	ns
		XC4020E	12.0	8.7	7.4	ns
		XC4025E	12.0	9.6	8.2	ns
T going Low to LL going from resistive pull-up or floating High to active Low. TBUF configured as open-drain or active buffer with I = Low. (Note1)	T_{ON}	XC4003E	5.5	4.6	3.9	ns
		XC4005E	7.0	6.0	5.4	ns
		XC4006E	7.5	6.7	5.7	ns
		XC4008E	8.0	7.1	6.0	ns
		XC4010E	8.5	7.3	6.2	ns
		XC4013E	8.7	7.5	6.4	ns
		XC4020E	11.0	8.4	7.1	ns
		XC4025E	11.0	8.4	7.1	ns
T going High to TBUF going inactive, not driving LL	T_{OFF}	All devices	1.8	1.5	1.3	ns
T going High to LL going from Low to High, pulled up by a single resistor. (Note 2)	T_{PUS}	XC4003E	20.0	14.0	11.9	ns
		XC4005E	23.0	16.0	13.6	ns
		XC4006E	25.0	18.0	15.3	ns
		XC4008E	27.0	20.0	17.0	ns
		XC4010E	29.0	22.0	18.7	ns
		XC4013E	32.0	26.0	22.1	ns
		XC4020E	35.0	32.5	27.6	ns
		XC4025E	42.0	39.1	33.2	ns
T going High to LL going from Low to High, pulled up by two resistors. (Note1)	T_{PUF}	XC4003E	9.0	7.0	6.0	ns
		XC4005E	10.0	8.0	6.8	ns
		XC4006E	11.5	9.0	7.7	ns
		XC4008E	12.5	10.0	8.5	ns
		XC4010E	13.5	11.0	9.4	ns
		XC4013E	15.0	13.0	11.0	ns
		XC4020E	16.0	14.8	12.6	ns
		XC4025E	18.0	16.5	14.0	ns
			PRELIMINARY		ADVANCE	

Note 1: These values include a minimum load. The values reported by LCA2XNF -S include only a portion of this delay, therefore the values cannot be directly compared. Use XDelay to determine the delay for each destination.

Note 2: This value includes a minimum load. The value reported by LCA2XNF -S is increased to allow for potentially heavy loading, therefore the values cannot be directly compared. Use XDelay to determine the delay for each destination.

XC4000E CLB Switching Characteristic Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are not measured directly. They are derived from benchmark timing patterns that are taken at device introduction, prior to any process improvements. For more detailed, more precise, and more up-to-date information, use the values provided by the XACT timing calculator and used in the simulator. These values can be printed in tabular format by running LCA2XNF -S.

The following guidelines reflect worst-case values over the recommended operating conditions. They are expressed in units of nanoseconds and apply to all XC4000E devices unless otherwise noted.

Speed Grade		-4		-3		-2	
Description	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**
Combinatorial Delays							
F/G inputs to X/Y outputs	T_{ILO}		2.7		2.0		1.6
F/G inputs via H' to X/Y outputs	T_{IHO}		4.7		4.3		2.7
C inputs via SR through H' to X/Y outputs	T_{HH0O}		4.1		3.3		2.4
C inputs via H' to X/Y outputs	T_{HH1O}		3.7		3.6		2.2
C inputs via DIN through H' to X/Y outputs	T_{HH2O}		4.5		3.6		2.6
CLB Fast Carry Logic							
Operand inputs (F1, F2, G1, G4) to COUT	T_{OPCY}		3.2		2.6		2.1
Add/Subtract input (F3) to COUT	T_{ASCY}		5.5		4.4		3.7
Initialization inputs (F1, F3) to COUT	T_{INCY}		1.7		1.7		1.4
CIN through function generators to X/Y outputs	T_{SUM}		3.8		3.3		2.6
CIN to COUT, bypass function generators	T_{BYP}		1.0		0.7		0.6
Sequential Delays							
Clock K to outputs Q	T_{CKO}		3.7		2.8		2.8
Setup Time before Clock K							
F/G inputs	T_{ICK}	4.0		3.0		2.4	
F/G inputs via H'	T_{IHCK}	6.1		4.6		3.9	
C inputs via H0 through H'	T_{HH0CK}	4.5		3.6		3.5	
C inputs via H1 through H'	T_{HH1CK}	5.0		4.1		3.3	
C inputs via H2 through H'	T_{HH2CK}	4.8		3.8		3.7	
C inputs via DIN	T_{DICK}	3.0		2.4		2.0	
C inputs via EC	T_{ECCK}	4.0		3.0		2.6	
C inputs via S/R, going Low (inactive)	T_{RCK}	4.2		4.0		4.0	
C_{IN} input via F'/G'	T_{CCK}						
C_{IN} input via F'/G' and H'	T_{CHCK}						
		PRELIMINARY				ADVANCE	

XC4000E CLB Switching Characteristic Guidelines (continued)

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are not measured directly. They are derived from benchmark timing patterns that are taken at device introduction, prior to any process improvements. For more detailed, more precise, and more up-to-date information, use the values provided by the XACT timing calculator and used in the simulator. These values can be printed in tabular format by running LCA2XNF -S.

The following guidelines reflect worst-case values over the recommended operating conditions. They are expressed in units of nanoseconds and apply to all XC4000E devices unless otherwise noted.

Speed Grade		-4		-3		-2	
Description	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**
Hold Time after Clock K							
F/G inputs	T_{CKI}	0		0		0	
F/G inputs via H'	T_{CKIH}	0		0		0	
C inputs via H0 through H'	T_{CKHH0}	0		0		0	
C inputs via H1 through H'	T_{CKHH1}	0		0		0	
C inputs via H2 through H'	T_{CKHH2}	0		0		0	
C inputs via DIN	T_{CKDI}	0		0		0	
C inputs via EC	T_{CKEC}	0		0		0	
C inputs via SR, going Low (inactive)	T_{CKR}	0		0		0	
Clock							
Clock High time	T_{CH}	4.5		4.0		4.0	
Clock Low time	T_{CL}	4.5		4.0		4.0	
Set/Reset Direct							
Width (High)	T_{RPW}	5.5		4.0		4.0	
Delay from C inputs via S/R, going High to Q	T_{RIO}		6.5		4.0		4.0
Master Set/Reset (Note 1)							
Width (High or Low)	T_{MRW}	13.0		11.5		11.5	
Delay from Global Set/Reset net to Q	T_{MRQ}		23.0		18.7		17.4
Global Set/Reset inactive to first active clock K edge	T_{MRK}						
Toggle Frequency[2] (MHz)	F_{TOG}		111		125		125
		PRELIMINARY				ADVANCE	

Notes: 1. Timing is based on the XC4005E. For other devices see the XACT timing calculator.
2. Export Control Max. flip-flop toggle rate.

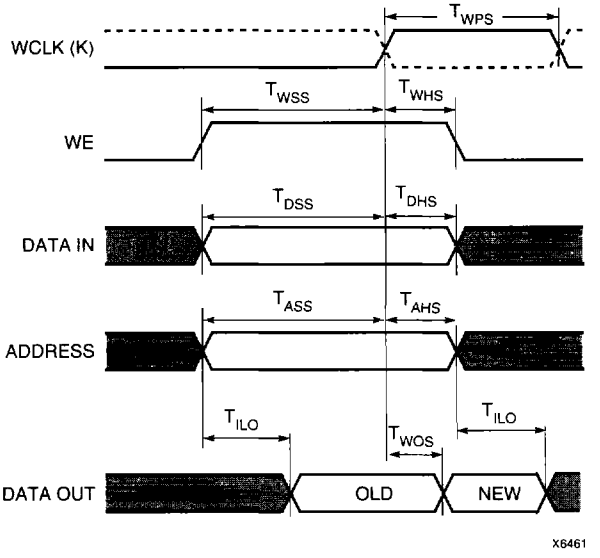
XC4000E CLB Edge-Triggered (Synchronous) RAM Switching Characteristic Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are not measured directly. They are derived from benchmark timing patterns that are taken at device introduction, prior to any process improvements. For more detailed, more precise, and more up-to-date information, use the values provided by the XACT timing calculator and used in the simulator. These values can be printed in tabular format by running LCA2XNF -S.

The following guidelines reflect worst-case values over the recommended operating conditions. They are expressed in units of nanoseconds and apply to all XC4000E devices unless otherwise noted.

Speed Grade			-4		-3		-2	
Description	**Size**	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**
Write Operation								
Address write cycle time	16x2	T_{WCS}	15.0		14.4		11.6	
(clock K period)	32x1	T_{WCTS}	15.0		14.4		11.6	
Clock K pulse width	16x2	T_{WPS}	7.5	1 ms	7.2	1 ms	5.8	1 ms
(active edge)	32x1	T_{WPTS}	7.5	1 ms	7.2	1 ms	5.8	1 ms
Address setup time	16x2	T_{ASS}	2.8		2.4		2.0	
before clock K	32x1	T_{ASTS}	2.8		2.4		2.0	
Address hold time	16x2	T_{AHS}	0		0		0	
after clock K	32x1	T_{AHTS}	0		0		0	
DIN setup time	16x2	T_{DSS}	3.5		3.2		2.7	
before clock K	32x1	T_{DSTS}	2.5		1.9		1.7	
DIN hold time	16x2	T_{DHS}	0		0		0	
after clock K	32x1	T_{DHTS}	0		0		0	
WE setup time	16x2	T_{WSS}	2.2		2.0		1.6	
before clock K	32x1	T_{WSTS}	2.2		2.0		1.6	
WE hold time	16x2	T_{WHS}	0		0		0	
after clock K	32x1	T_{WHTS}	0		0		0	
Data valid	16x2	T_{WOS}		10.3		8.8		6.3
after clock K	32x1	T_{WOTS}		11.6		10.3		7.4
			PRELIMINARY				ADVANCE	

Note 1: Timing for the 16x1 RAM option is identical to 16x2 RAM timing.
Note 2: Applicable Read timing specifications are identical to Level-Sensitive Read timing.



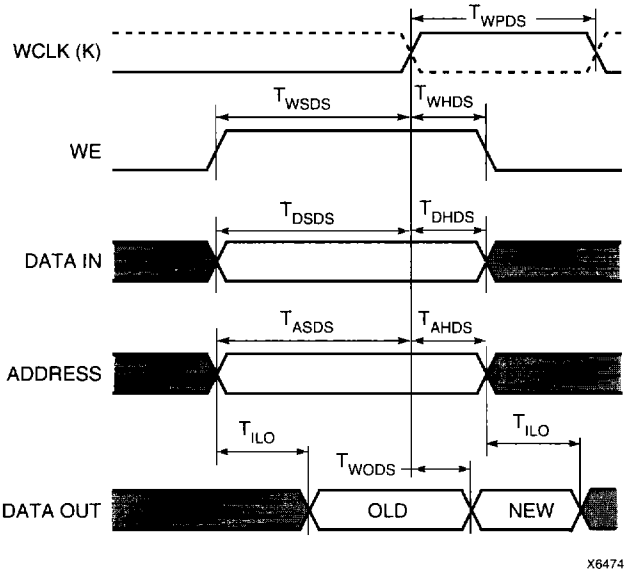
XC4000E CLB Edge-Triggered (Synchronous) Dual-Port RAM Switching Characteristic Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are not measured directly. They are derived from benchmark timing patterns that are taken at device introduction, prior to any process improvements. For more detailed, more precise, and more up-to-date information, use the values provided by the XACT timing calculator and used in the simulator. These values can be printed in tabular format by running LCA2XNF -S.

The following guidelines reflect worst-case values over the recommended operating conditions. They are expressed in units of nanoseconds and apply to all XC4000E devices unless otherwise noted.

	Speed Grade		-4		-3		-2	
Description	**Size**	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**
Write Operation								
Address write cycle time (clock K period)	16x1	T_{WCDS}	15.0		14.4		11.6	
Clock K pulse width (active edge)	16x1	T_{WPDS}	7.5	1 ms	7.2	1 ms	5.8	1 ms
Address setup time before clock K	16x1	T_{ASDS}	2.8		2.5		2.1	
Address hold time after clock K	16x1	T_{AHDS}	0		0		0	
DIN setup time before clock K	16x1	T_{DSDS}	2.2		1.9		1.6	
DIN hold time after clock K	16x1	T_{DHDS}	0		0		0	
WE setup time before clock K	16x1	T_{WSDS}	2.2		2.0		1.6	
WE hold time after clock K	16x1	T_{WHDS}	0.3		0		0	
Data valid after clock K	16x1	T_{WODS}		10.0		7.8		6.2
			PRELIMINARY				ADVANCE	

Note: Applicable Read timing specifications are identical to16x2 Level-Sensitive Read timing.



XC4000E CLB Level-Sensitive RAM Switching Characteristic Guidelines

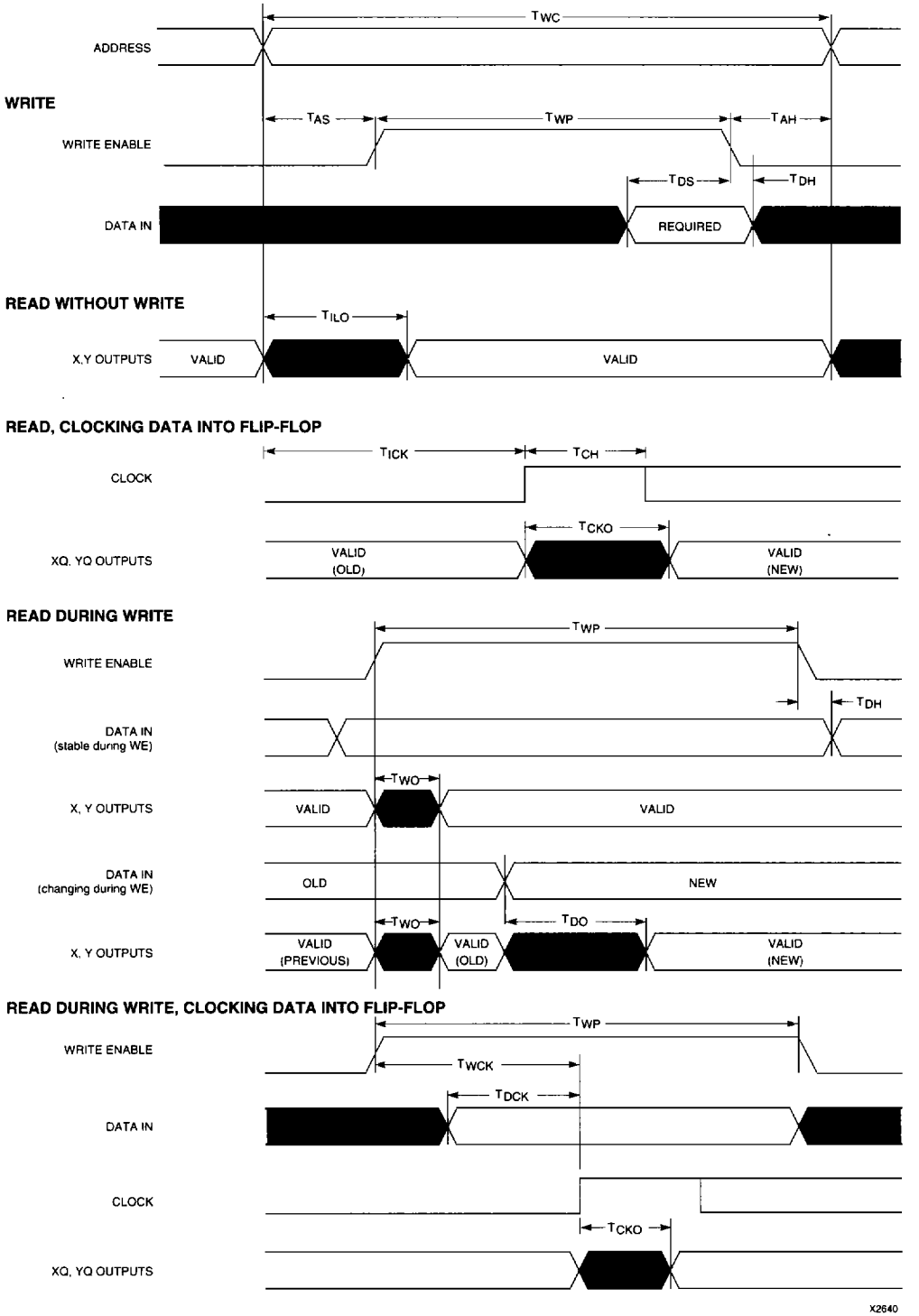
Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are not measured directly. They are derived from benchmark timing patterns that are taken at device introduction, prior to any process improvements. For more detailed, more precise, and more up-to-date information, use the values provided by the XACT timing calculator and used in the simulator. These values can be printed in tabular format by running LCA2XNF -S.

The following guidelines reflect worst-case values over the recommended operating conditions. They are expressed in units of nanoseconds and apply to all XC4000E devices unless otherwise noted.

Speed Grade			-4		-3		-2	
Description	**Size**	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**
Write Operation								
Address write cycle time	16x2	T_{WC}	8.0		8.0		8.0	
	32x1	T_{WCT}	8.0		8.0		8.0	
Write Enable pulse width	16x2	T_{WP}	4.0		4.0		4.0	
(High)	32x1	T_{WPT}	4.0		4.0		4.0	
Address setup time	16x2	T_{AS}	2.0		2.0		2.0	
before WE	32x1	T_{AST}	2.0		2.0		2.0	
Address hold time	16x2	T_{AH}	2.5		2.0		2.0	
after end of WE	32x1	T_{AHT}	2.0		2.0		2.0	
DIN setup time	16x2	T_{DS}	4.0		2.2		0.8	
before end of WE	32x1	T_{DST}	5.0		2.2		0.8	
DIN hold time	16x2	T_{DH}	2.0		2.0		2.0	
after end of WE	32x1	T_{DHT}	2.0		2.0		2.0	
Read Operation								
Address read cycle time	16x2	T_{RC}	4.5		3.1		2.6	
	32x1	T_{RCT}	6.5		5.5		3.8	
Data valid after address	16x2	T_{ILO}		2.7		2.0		1.6
change (no Write Enable)	32x1	T_{IHO}		4.7		4.3		2.7
Read Operation, Clocking Data into Flip-Flop								
Address setup time	16x2	T_{ICK}	4.0		3.0		2.4	
before clock K	32x1	T_{IHCK}	6.1		4.6		3.9	
Read During Write								
Data valid after WE goes	16x2	T_{WO}		10.0		6.0		4.9
active (DIN stable	32x1	T_{WOT}		12.0		7.3		5.6
before WE)								
Data valid after DIN	16x2	T_{DO}		9.0		6.6		5.8
(DIN changes during WE)	32x1	T_{DOT}		11.0		7.6		6.2
Read During Write, Clocking Data into Flip-Flop								
WE setup time	16x2	T_{WCK}	8.0		6.0		5.1	
before clock K	32x1	T_{WCKT}	9.6		6.8		5.8	
Data setup time	16x2	T_{DCK}	7.0		5.2		4.4	
before clock K	32x1	T_{DCKT}	8.0		6.2		5.3	
			PRELIMINARY				ADVANCE	

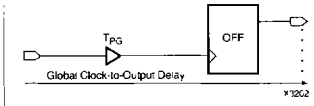
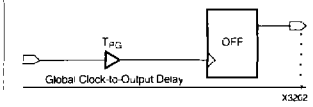
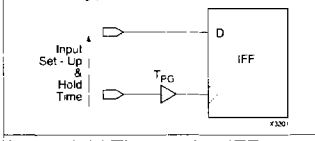
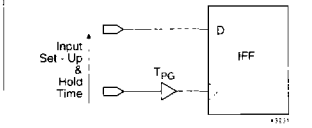
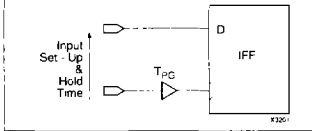
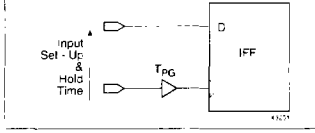
Note: Timing for the 16x1 RAM option is identical to 16x2 RAM timing.

XC4000E CLB Level-Sensitive RAM Timing Characteristics



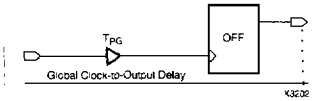
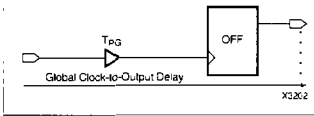
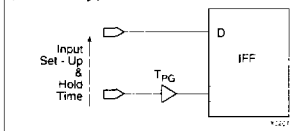
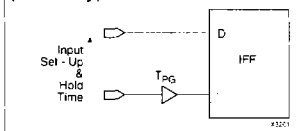
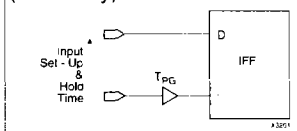
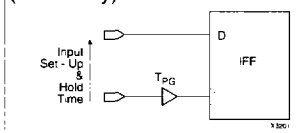
XC4000E Guaranteed Input and Output Parameters (Pin-to-Pin, TTL Inputs)

All values listed below are tested directly, and guaranteed over the operating conditions. The same parameters can also be derived indirectly from the IOB and Global Buffer specifications. The XACT delay calculator uses this indirect method. When there is a discrepancy between the two methods, the values listed below should be used, and the derived values must be ignored. All values are expressed in units of nanoseconds.

		Speed Grade	-4	-3	-2
Description	**Symbol**	**Device**			
Global Clock to Output (fast) using OFF 	T_{ICKOF} (Max)	XC4003E	12.5	10.2	8.7
		XC4005E	14.0	10.7	9.1
		XC4006E	14.5	10.7	9.1
		XC4008E	15.0	10.8	9.2
		XC4010E	16.0	10.9	9.3
		XC4013E	16.5	11.0	9.4
		XC4020E	17.0	11.0	9.4
		XC4025E	17.0	12.6	10.7
Global Clock to Output (slew-limited) using OFF 	T_{ICKO} (Max)	XC4003E	16.5	14.0	11.5
		XC4005E	18.0	14.7	12.0
		XC4006E	18.5	14.7	12.0
		XC4008E	19.0	14.8	12.1
		XC4010E	20.0	14.9	12.2
		XC4013E	20.5	15.0	12.8
		XC4020E	21.0	15.1	12.8
		XC4025E	21.0	15.3	13.0
Input Setup Time, using IFF (no delay) 	T_{PSUF} (Min)	XC4003E	2.5	2.3	2.3
		XC4005E	2.0	1.2	1.2
		XC4006E	1.9	1.0	1.0
		XC4008E	1.4	0.6	0.6
		XC4010E	1.0	0.2	0.2
		XC4013E	0.5	0	0
		XC4020E	0	0	0
		XC4025E	0	0	0
Input Hold Time, using IFF (no delay) 	T_{PHF} (Min)	XC4003E	4.0	4.0	4.0
		XC4005E	4.6	4.5	4.5
		XC4006E	5.0	4.7	4.7
		XC4008E	6.0	5.1	5.1
		XC4010E	6.0	5.5	5.5
		XC4013E	7.0	6.5	5.5
		XC4020E	7.5	6.7	5.7
		XC4025E	8.0	7.0	5.9
Input Setup Time, using IFF (with delay) 	T_{PSU} (Min)	XC4003E	8.5	7.0	6.0
		XC4005E	8.5	7.0	6.0
		XC4006E	8.5	7.0	6.0
		XC4008E	8.5	7.0	6.0
		XC4010E	8.5	7.0	6.0
		XC4013E	8.5	7.0	6.0
		XC4020E	9.5	7.0	6.0
		XC4025E	9.5	7.6	6.5
Input Hold Time, using IFF (with delay) 	T_{PH} (Min)	XC4003E	0	0	0
		XC4005E	0	0	0
		XC4006E	0	0	0
		XC4008E	0	0	0
		XC4010E	0	0	0
		XC4013E	0	0	0
		XC4020E	0	0	0
		XC4025E	0	0	0
OFF = Output Flip-Flop	IFF = Input Flip-Flop or Latch		PRELIMINARY		ADVANCE

XC4000E Guaranteed Input and Output Parameters (Pin-to-Pin, CMOS Inputs)

All values listed below are tested directly, and guaranteed over the operating conditions. The same parameters can also be derived indirectly from the IOB and Global Buffer specifications. The XACT delay calculator uses this indirect method. When there is a discrepancy between the two methods, the values listed below should be used, and the derived values must be ignored. All values are expressed in units of nanoseconds.

Description	Symbol	Speed Grade: Device	-4	-3	-2	
Global Clock to Output (fast) using OFF 	T_{ICKOF} (Max)	XC4003E XC4005E XC4006E XC4008E XC4010E XC4013E XC4020E XC4025E				
Global Clock to Output (slew-limited) using OFF 	T_{ICKO} (Max)	XC4003E XC4005E XC4006E XC4008E XC4010E XC4013E XC4020E XC4025E				
Input Setup Time, using IFF (no delay) 	T_{CPSUF} (Min)	XC4003E XC4005E XC4006E XC4008E XC4010E XC4013E XC4020E XC4025E				
Input Hold Time, using IFF (no delay) 	T_{CPHF} (Min)	XC4003E XC4005E XC4006E XC4008E XC4010E XC4013E XC4020E XC4025E				
Input Setup Time, using IFF (with delay) 	T_{CPSU} (Min)	XC4003E XC4005E XC4006E XC4008E XC4010E XC4013E XC4020E XC4025E				
Input Hold Time, using IFF (with delay) 	T_{CPH} (Min)	XC4003E XC4005E XC4006E XC4008E XC4010E XC4013E XC4020E XC4025E				
OFF = Output Flip-Flop	IFF = Input Flip-Flop or Latch		PRELIMINARY		ADVANCE	

XC4000E IOB Input Switching Characteristic Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are not measured directly. They are derived from benchmark timing patterns that are taken at device introduction, prior to any process improvements. For more detailed, more precise, and more up-to-date information, use the values provided by the XACT timing calculator and used in the simulator. These values can be printed in tabular format by running LCA2XNF -S.

The following guidelines reflect worst-case values over the recommended operating conditions. They are expressed in units of nanoseconds and apply to all XC4000E devices unless otherwise noted.

	Speed Grade		-4		-3		-2	
Description	**Symbol**	**Device**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**
Propagation Delays (TTL Inputs)								
Pad to I1, I2	T_{PID}	All devices		3.0		2.5		2.0
Pad to I1, I2 via transparent latch,	T_{PLI}	All devices		4.8		3.6		3.6
no delay	T_{PDLI}	XC4003E		10.4		9.3		7.0
with delay		XC4005E		10.8		9.6		7.3
		XC4006E		10.8		10.2		7.8
		XC4008E		10.8		10.6		8.1
		XC4010E		11.0		10.8		8.2
		XC4013E		11.4		11.2		8.5
		XC4020E		13.8		12.4		9.5
		XC4025E		13.8		13.7		9.5
(CMOS Inputs)								
Pad to I1, I2	T_{PIDC}	All devices		5.5		4.1		3.7
Pad to I1, I2 via transparent latch,	T_{PLIC}	All devices		8.8		6.8		6.2
no delay	T_{PDLIC}	XC4003E		16.5		12.4		11.0
with delay		XC4005E		16.5		13.2		11.9
		XC4006E		16.8		13.4		12.1
		XC4008E		17.3		13.8		12.4
		XC4010E		17.5		14.0		12.6
		XC4013E		18.0		14.4		13.0
		XC4020E		20.8		15.6		14.0
		XC4025E		20.8		15.6		14.0
(TTL or CMOS)								
Clock (IK) to I1, I2 (flip-flop)	T_{IKRI}	All devices		5.6		2.8		2.8
Clock (IK) to I1, I2 (latch enable, active Low)	T_{IKLI}	All devices		6.2		4.0		3.9
Hold Times (Note 1)								
Pad to Clock (IK), no delay	T_{IKPI}	All devices	0		0		0	
with delay	T_{IKPID}	All devices	0		0		0	
Clock Enable (EC) to Clock (IK)								
no delay	T_{IKEC}	All devices	1.5		1.5		0.9	
with delay	T_{IKECD}	All devices	0		0		0	
			PRELIMINARY				ADVANCE	

Note 1: Input pad setup and hold times are specified with respect to the internal clock (IK). For setup and hold times with respect to the clock input pin, see the pin-to-pin parameters in the Guaranteed Input and Output Parameters table.

Note 2: Voltage levels of unused pads, bonded or unbonded, must be valid logic levels. Each can be configured with the internal pull-up (default) or pull-down resistor, or configured as a driven output, or can be driven from an external source.

XC4000E IOB Input Switching Characteristic Guidelines (continued)

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are not measured directly. They are derived from benchmark timing patterns that are taken at device introduction, prior to any process improvements. For more detailed, more precise, and more up-to-date information, use the values provided by the XACT timing calculator and used in the simulator. These values can be printed in tabular format by running LCA2XNF -S.

The following guidelines reflect worst-case values over the recommended operating conditions. They are expressed in units of nanoseconds and apply to all XC4000E devices unless otherwise noted.

	Speed Grade		-4		-3		-2			
Description	**Symbol**	**Device**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**		
Setup Times (TTL Inputs)										
Pad to Clock (IK), no delay	T_{PICK}	All devices	4.0		2.6		1.7			
with delay	T_{PICKD}	XC4003E	10.9		8.2		5.5			
		XC4005E	10.9		8.7		5.5			
		XC4006E	10.9		9.2		6.6			
		XC4008E	11.1		9.6		6.9			
		XC4010E	11.3		9.8		7.0			
		XC4013E	11.8		10.2		7.3			
		XC4020E	14.0		11.4		8.2			
		XC4025E	14.0		11.4		8.2			
(CMOS Inputs)										
Pad to Clock (IK), no delay	T_{PICKC}	All devices	6.0		3.3		2.4			
with delay	T_{PICKDC}	XC4003E	12.0		8.8		6.2			
		XC4005E	12.0		9.7		6.2			
		XC4006E	12.3		9.9		7.3			
		XC4008E	12.8		10.3		7.6			
		XC4010E	13.0		10.5		7.7			
		XC4013E	13.5		10.9		8.0			
		XC4020E	16.0		12.1		8.9			
		XC4025E	16.0		12.1		8.9			
(TTL or CMOS)										
Clock Enable (EC) to Clock (IK),	T_{ECIK}	All devices	3.5		2.5		2.0			
no delay	T_{ECIKD}	XC4003E	10.4		8.1		5.6			
with delay		XC4005E	10.4		8.5		5.6			
		XC4006E	10.4		9.1		6.9			
		XC4008E	10.4		9.5		7.2			
		XC4010E	10.7		9.7		7.3			
		XC4013E	11.1		10.1		7.6			
		XC4020E	14.0		11.3		8.5			
		XC4025E	14.0		11.3		8.5			
Global Set/Reset (Note 3)										
Delay from GSR net through Q to I1, I2	T_{RRI}			12.0		7.8		6.8		
GSR width	T_{MRW}		13.0		11.5		11.5			
GSR inactive to first active Clock (IK) edge	T_{MRI}									
			PRELIMINARY				ADVANCE			

Note 1: Input pad setup and hold times are specified with respect to the internal clock (IK). For setup and hold times with respect to the clock input pin. see the pin-to-pin parameters in the Guaranteed Input and Output Parameters table.

Note 2: Voltage levels of unused pads, bonded or unbonded, must be valid logic levels. Each can be configured with the internal pull-up (default) or pull-down resistor, or configured as a driven output, or can be driven from an external source.

Note 3: Timing is based on the XC4005E. For other devices see the XACT timing calculator.

XC4000E IOB Output Switching Characteristic Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are not measured directly. They are derived from benchmark timing patterns that are taken at device introduction, prior to any process improvements. For more detailed, more precise, and more up-to-date information, use the values provided by the XACT timing calculator and used in the simulator. These values can be printed in tabular format by running LCA2XNF -S.

The following guidelines reflect worst-case values over the recommended operating conditions. They are expressed in units of nanoseconds and apply to all XC4000E devices unless otherwise noted.

Speed Grade		-4		-3		-2	
Description	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**
Propagation Delays (TTL Output Levels)							
Clock (OK) to Pad, fast	T_{OKPOF}		7.5		6.5		4.5
slew-rate limited	T_{OKPOS}		11.5		9.5		7.0
Output (O) to Pad, fast	T_{OPF}		8.0		5.5		4.8
slew-rate limited	T_{OPS}		12.0		8.5		7.3
3-state to Pad hi-Z (slew-rate independent)	T_{TSHZ}		5.0		4.2		3.8
3-state to Pad active and valid, fast	T_{TSONF}		9.7		8.1		7.3
slew-rate limited	T_{TSONS}		13.7		11.1		9.8
Propagation Delays (CMOS Output Levels)							
Clock (OK) to Pad, fast	T_{OKPOFC}		9.5		7.8		7.0
slew-rate limited	T_{OKPOSC}		13.5		11.6		10.4
Output (O) to Pad, fast	T_{OPFC}		10.0		9.7		8.7
slew-rate limited	T_{OPSC}		14.0		13.4		12.1
3-state to Pad hi-Z (slew-rate independent)	T_{TSHZC}		5.2		4.3		3.9
3-state to Pad active and valid, fast	T_{TSONFC}		9.1		7.6		6.8
slew-rate limited	T_{TSONSC}		13.1		11.4		10.2
		PRELIMINARY				ADVANCE	

Note 1: Output timing is measured at pin threshold, with 50pF external capacitive loads (incl. test fixture). Slew-rate limited output rise/fall times are approximately two times longer than fast output rise/fall times. For the effect of capacitive loads on ground bounce, see the "Additional XC4000 Data" section of the Programmable Logic Data Book.

Note 2: Voltage levels of unused pads, bonded or unbonded, must be valid logic levels. Each can be configured with the internal pull-up (default) or pull-down resistor, or configured as a driven output, or can be driven from an external source.

XC4000E IOB Output Switching Characteristic Guidelines (continued)

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are not measured directly. They are derived from benchmark timing patterns that are taken at device introduction, prior to any process improvements. For more detailed, more precise, and more up-to-date information, use the values provided by the XACT timing calculator and used in the simulator. These values can be printed in tabular format by running LCA2XNF -S.

The following guidelines reflect worst-case values over the recommended operating conditions. They are expressed in units of nanoseconds and apply to all XC4000E devices unless otherwise noted.

Speed Grade		-4		-3		-2	
Description	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**
Setup and Hold							
Output (O) to clock (OK) setup time	T_{OOK}	5.0		4.6		3.8	
Output (O) to clock (OK) hold time	T_{OKO}	0		0		0	
Clock Enable (EC) to clock (OK) setup	T_{ECOK}	4.8		3.5		2.5	
Clock Enable (EC) to clock (OK) hold	T_{OKEC}	1.2		1.2		0.5	
Clock							
Clock High	T_{CH}	4.5		4.0		4.0	
Clock Low	T_{CL}	4.5		4.0		4.0	
Global Set/Reset (Note 3)							
Delay from GSR net to Pad	T_{RPO}		15.0		11.8		8.7
GSR width	T_{MRW}	13.0		11.5		11.5	
GSR inactive to first active clock (OK) edge	T_{MRO}						
		PRELIMINARY				ADVANCE	

Note 1: Output timing is measured at pin threshold, with 50pF external capacitive loads (incl. test fixture). Slew-rate limited output rise/fall times are approximately two times longer than fast output rise/fall times. For the effect of capacitive loads on ground bounce, see the "Additional XC4000 Data" section of the Programmable Logic Data Book.

Note 2: Voltage levels of unused pads, bonded or unbonded, must be valid logic levels. Each can be configured with the internal pull-up (default) or pull-down resistor, or configured as a driven output, or can be driven from an external source.

Note 3: Timing is based on the XC4005E. For other devices see the XACT timing calculator.

XC4000E Boundary Scan (JTAG) Switching Characteristic Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are not measured directly. They are derived from benchmark timing patterns that are taken at device introduction, prior to any process improvements. For more detailed, more precise, and more up-to-date information, use the values provided by the XACT timing calculator and used in the simulator. These values can be printed in tabular format by running LCA2XNF -S.

The following guidelines reflect worst-case values over the recommended operating conditions. They are expressed in units of nanoseconds and apply to all XC4000E devices unless otherwise noted.

Speed Grade		-4		-3		-2			
Description	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**		
Setup and Hold									
Input (TDI) to clock (TCK) setup time	T_{TDITCK}								
Input (TDI) to clock (TCK) hold time	T_{TCKTDI}								
Input (TMS) to clock (TCK) setup time	T_{TMSTCK}								
Input (TMS) to clock (TCK) hold time	T_{TCKTMS}								
Propagation Delay									
Clock (TCK) to Pad (TDO)	T_{TCKPO}								
Clock									
Clock (TCK) High	T_{TCKH}								
Clock (TCK) Low	T_{TCKL}								
Power-On Reset									
JTAG operation after valid Vcc	T_{RJTAG}								
		PRELIMINARY				ADVANCE			

Note 1: Input pad setup and hold times are specified with respect to the internal clock (IK). For setup and hold times with respect to the clock input pin, see the pin-to-pin parameters in the Guaranteed Input and Output Parameters table.

Note 2: Output timing is measured at pin threshold, with 50pF external capacitive loads (incl. test fixture). Slew-rate limited output rise/fall times are approximately two times longer than fast output rise/fall times. For the effect of capacitive loads on ground bounce, see the "Additional XC4000 Data" section of the Programmable Logic Data Book.

Note 3: Voltage levels of unused pads, bonded or unbonded, must be valid logic levels. Each can be configured with the internal pull-up (default) or pull-down resistor, or configured as a driven output, or can be driven from an external source.

XC4000L Switching Characteristics

XC4000L timing parameters were not available at the time this document was released. See the Xilinx WEBLINX at http://www.xilinx.com for the latest available information.

XC4000EX Switching Characteristics

XC4000EX timing parameters were not available at the time this document was released. See the Xilinx WEBLINX at http://www.xilinx.com for the latest available information.

XC4000XL Switching Characteristics

XC4000XL timing parameters were not available at the time this document was released. See the Xilinx WEBLINX at http://www.xilinx.com for the latest available information.

Device-Specific Pinout Tables

Pin Locations for XC4003E Devices

XC4003E Pad Name	PC 84	PQ 100	VQ 100	PG 120	Bndry Scan
VCC	P2	P92	P89	G3	-
I/O (A8)	P3	P93	P90	G1	32
I/O (A9)	P4	P94	P91	F1	35
I/O	-	P95	P92	E1	38
I/O	-	P96	P93	F2	41
I/O (A10)	P5	P97	P94	F3	44
I/O (A11)	P6	P98	P95	D1	47
I/O (A12)	P7	P99	P96	C1	50
I/O (A13)	P8	P100	P97	D2	53
I/O (A14)	P9	P1	P98	C2	56
I/O, SGCK1 (A15)	P10	P2	P99	D3	59
VCC	P11	P3	P100	C3	-
GND	P12	P4	P1	C4	-
I/O, PGCK1 (A16)	P13	P5	P2	B2	62
I/O (A17)	P14	P6	P3	B3	65
I/O, TDI	P15	P7	P4	C5	68
I/O, TCK	P16	P8	P5	B4	71
I/O, TMS	P17	P9	P6	B5	74
I/O	P18	P10	P7	A4	77
I/O	-	-	-	C6	80
I/O	-	P11	P8	A5	83
I/O	P19	P12	P9	B6	86
I/O	P20	P13	P10	A6	89
GND	P21	P14	P11	B7	-
VCC	P22	P15	P12	C7	-
I/O	P23	P16	P13	A7	92
I/O	P24	P17	P14	A8	95
I/O	-	P18	P15	A9	98
I/O	-	-	-	B8	101
I/O	P25	P19	P16	C8	104
I/O	P26	P20	P17	A10	107
I/O	P27	P21	P18	B9	110
I/O	-	P22	P19	A11	113
I/O	P28	P23	P20	C9	116
I/O, SCGK2	P29	P24	P21	A12	119
O (M1)	P30	P25	P22	B11	122
GND	P31	P26	P23	C10	-
I (M0)	P32	P27	P24	C11	125
VCC	P33	P28	P25	D11	-
I (M2)	P34	P29	P26	B12	126
I/O, PGCK2	P35	P30	P27	C12	127
I/O (HDC)	P36	P31	P28	A13	130
I/O	-	P32	P29	D12	133
I/O (LDC)	P37	P33	P30	C13	136
I/O	P38	P34	P31	E12	139
I/O	P39	P35	P32	D13	142
I/O	-	P36	P33	F11	145
I/O	-	P37	P34	E13	148
I/O	P40	P38	P35	F12	151
I/O (INIT)	P41	P39	P36	F13	154
VCC	P42	P40	P37	G12	-
GND	P43	P41	P38	G11	-
I/O	P44	P42	P39	G13	157
I/O	P45	P43	P40	H13	160
I/O	-	P44	P41	J13	163
I/O	-	P45	P42	H12	166
I/O	P46	P46	P43	H11	169
I/O	P47	P47	P44	K13	172
I/O	P48	P48	P45	J12	175
I/O	P49	P49	P46	L13	178
I/O	P50	P50	P47	M13	181
I/O, SGCK3	P51	P51	P48	L12	184
GND	P52	P52	P49	K11	-
DONE	P53	P53	P50	L11	-
VCC	P54	P54	P51	L10	-
PROGRAM	P55	P55	P52	M12	-
I/O (D7)	P56	P56	P53	M11	187
I/O, PGCK3	P57	P57	P54	N13	190
I/O (D6)	P58	P58	P55	M10	193
I/O	-	P59	P56	N11	196
I/O (D5)	P59	P60	P57	M9	199
I/O ($\overline{CS0}$)	P60	P61	P58	N10	202
I/O	-	P62	P59	L8	205
I/O	-	P63	P60	N9	208
I/O (D4)	P61	P64	P61	M8	211
I/O	P62	P65	P62	N8	214
VCC	P63	P66	P63	M7	-
GND	P64	P67	P64	L7	-
I/O (D3)	P65	P68	P65	N7	217
I/O ($\overline{RS}$)	P66	P69	P66	N6	220
I/O	-	P70	P67	N5	223
I/O	-	-	-	M6	226
I/O (D2)	P67	P71	P68	L6	229
I/O	P68	P72	P69	N4	232
I/O (D1)	P69	P73	P70	M5	235
I/O ($\overline{RCLK}$, RDY/$\overline{BUSY}$)	P70	P74	P71	N3	238
I/O (D0, DIN)	P71	P75	P72	N2	241
I/O, SGCK4 (DOUT)	P72	P76	P73	M3	244
CCLK	P73	P77	P74	L4	-
VCC	P74	P78	P75	L3	-
O, TDO	P75	P79	P76	M2	0
GND	P76	P80	P77	K3	-
I/O (A0, $\overline{WS}$)	P77	P81	P78	L2	2
I/O, PGCK4 (A1)	P78	P82	P79	N1	5
I/O (CS1, A2)	P79	P83	P80	K2	8
I/O (A3)	P80	P84	P81	L1	11
I/O (A4)	P81	P85	P82	J2	14
I/O (A5)	P82	P86	P83	K1	17
I/O	-	P87	P84	H3	20
I/O	-	P88	P85	J1	23
I/O (A6)	P83	P89	P86	H2	26
I/O (A7)	P84	P90	P87	H1	29
GND	P1	P91	P88	G2	-

4/2/96

Additional No Connect (N.C.) Connections on PG120 Package

PG120	PG120	PG120	PG120
A1	B13	J11	M4
A2	E2	K12	N12
A3	E3	L5	
B1	E11	L9	
B10	J3	M1	

2/28/96

Pin Locations for XC4005E/L Devices

XC4005 E/L Pad Name	PC 84	PQ 100	TQ 144	PG 156	PQ 160	PQ 208	Bndry Scan
VCC	P2	P92	P128	H3	P142	P183	-
I/O (A8)	P3	P93	P129	H1	P143	P184	44
I/O (A9)	P4	P94	P130	G1	P144	P185	47
I/O	-	P95	P131	G2	P145	P186	50
I/O	-	P96	P132	G3	P146	P187	53
I/O (A10)	P5	P97	P133	F1	P147	P190	56
I/O (A11)	P6	P98	P134	F2	P148	P191	59
I/O	-	-	P135	E1	P149	P192	62
I/O	-	-	P136	E2	P150	P193	65
GND	-	-	P137	F3	P151	P194	-
I/O (A12)	P7	P99	P138	E3	P154	P199	68
I/O (A13)	P8	P100	P139	C1	P155	P200	71
I/O	-	-	P140	C2	P156	P201	74
I/O	-	-	P141	D3	P157	P202	77
I/O (A14)	P9	P1	P142	B1	P158	P203	80
I/O, SGCK1 (A15)	P10	P2	P143	B2	P159	P204	83
VCC	P11	P3	P144	C3	P160	P205	-
GND	P12	P4	P1	C4	P1	P2	-
I/O, PGCK1 (A16)	P13	P5	P2	B3	P2	P4	86
I/O (A17)	P14	P6	P3	A1	P3	P5	89
I/O	-	-	P4	A2	P4	P6	92
I/O	-	-	P5	C5	P5	P7	95
I/O, TDI	P15	P7	P6	B4	P6	P8	98
I/O, TCK	P16	P8	P7	A3	P7	P9	101
GND	-	-	P8	C6	P10	P14	-
I/O	-	-	P9	B5	P11	P15	104
I/O	-	-	P10	B6	P12	P16	107
I/O, TMS	P17	P9	P11	A5	P13	P17	110
I/O	P18	P10	P12	C7	P14	P18	113
I/O	-	-	P13	B7	P15	P21	116
I/O	-	P11	P14	A6	P16	P22	119
I/O	P19	P12	P15	A7	P17	P23	122
I/O	P20	P13	P16	A8	P18	P24	125
GND	P21	P14	P17	C8	P19	P25	-
VCC	P22	P15	P18	B8	P20	P26	-
I/O	P23	P16	P19	C9	P21	P27	128
I/O	P24	P17	P20	B9	P22	P28	131
I/O	-	P18	P21	A9	P23	P29	134
I/O	-	-	P22	B10	P24	P30	137
I/O	P25	P19	P23	C10	P25	P33	140
I/O	P26	P20	P24	A10	P26	P34	143
I/O	-	-	P25	A11	P27	P35	146
I/O	-	-	P26	B11	P28	P36	149

XC4005 E/L Pad Name	PC 84	PQ 100	TQ 144	PG 156	PQ 160	PQ 208	Bndry Scan
GND	-	-	P27	C11	P29	P37	-
I/O	P27	P21	P28	B12	P32	P42	152
I/O	-	P22	P29	A13	P33	P43	155
I/O	-	-	P30	A14	P34	P44	158
I/O	-	-	P31	C12	P35	P45	161
I/O	P28	P23	P32	B13	P36	P46	164
I/O, SCGK2	P29	P24	P33	B14	P37	P47	167
O (M1)	P30	P25	P34	A15	P38	P48	170
GND	P31	P26	P35	C13	P39	P49	-
I (M0)	P32	P27	P36	A16	P40	P50	173
VCC	P33	P28	P37	C14	P41	P55	-
I (M2)	P34	P29	P38	B15	P42	P56	174
I/O, PGCK2	P35	P30	P39	B16	P43	P57	175
I/O (HDC)	P36	P31	P40	D14	P44	P58	178
I/O	-	-	P41	C15	P45	P59	181
I/O	-	-	P42	D15	P46	P60	184
I/O	-	P32	P43	E14	P47	P61	187
I/O ($\overline{\text{LDC}}$)	P37	P33	P44	C16	P48	P62	190
GND	-	-	P45	F14	P51	P67	-
I/O	-	-	P46	F15	P52	P68	193
I/O	-	-	P47	E16	P53	P69	196
I/O	P38	P34	P48	F16	P54	P70	199
I/O	P39	P35	P49	G14	P55	P71	202
I/O	-	P36	P50	G15	P56	P74	205
I/O	-	P37	P51	G16	P57	P75	208
I/O	P40	P38	P52	H16	P58	P76	211
I/O ($\overline{\text{INIT}}$)	P41	P39	P53	H15	P59	P77	214
VCC	P42	P40	P54	H14	P60	P78	-
GND	P43	P41	P55	J14	P61	P79	-
I/O	P44	P42	P56	J15	P62	P80	217
I/O	P45	P43	P57	J16	P63	P81	220
I/O	-	P44	P58	K16	P64	P82	223
I/O	-	P45	P59	K15	P65	P83	226
I/O	P46	P46	P60	K14	P66	P86	229
I/O	P47	P47	P61	L16	P67	P87	232
I/O	-	-	P62	M16	P68	P88	235
I/O	-	-	P63	L15	P69	P89	238
GND	-	-	P64	L14	P70	P90	-
I/O	P48	P48	P65	P16	P73	P95	241
I/O	P49	P49	P66	M14	P74	P96	244
I/O	-	-	P67	N15	P75	P97	247
I/O	-	-	P68	P15	P76	P98	250
I/O	P50	P50	P69	N14	P77	P99	253
I/O, SGCK3	P51	P51	P70	R16	P78	P100	256
GND	P52	P52	P71	P14	P79	P101	-

XC4005 E/L Pad Name	PC 84	PQ 100	TQ 144	PG 156	PQ 160	PQ 208	Bndry Scan
DONE	P53	P53	P72	R15	P80	P103	-
VCC	P54	P54	P73	P13	P81	P106	-
$\overline{\text{PRO-}}$ $\overline{\text{GRAM}}$	P55	P55	P74	R14	P82	P108	-
I/O (D7)	P56	P56	P75	T16	P83	P109	259
I/O, PGCK3	P57	P57	P76	T15	P84	P110	262
I/O	-	-	P77	R13	P85	P111	265
I/O	-	-	P78	P12	P86	P112	268
I/O (D6)	P58	P58	P79	T14	P87	P113	271
I/O	-	P59	P80	T13	P88	P114	274
GND	-	-	P81	P11	P91	P119	-
I/O	-	-	P82	R11	P92	P120	277
I/O	-	-	P83	T11	P93	P121	280
I/O (D5)	P59	P60	P84	T10	P94	P122	283
I/O ($\overline{\text{CS0}}$)	P60	P61	P85	P10	P95	P123	286
I/O	-	P62	P86	R10	P96	P126	289
I/O	-	P63	P87	T9	P97	P127	292
I/O (D4)	P61	P64	P88	R9	P98	P128	295
I/O	P62	P65	P89	P9	P99	P129	298
VCC	P63	P66	P90	R8	P100	P130	-
GND	P64	P67	P91	P8	P101	P131	-
I/O (D3)	P65	P68	P92	T8	P102	P132	301
I/O ($\overline{\text{RS}}$)	P66	P69	P93	T7	P103	P133	304
I/O	-	P70	P94	T6	P104	P134	307
I/O	-	-	P95	R7	P105	P135	310
I/O (D2)	P67	P71	P96	P7	P106	P138	313
I/O	P68	P72	P97	T5	P107	P139	316
I/O	-	-	P98	R6	P108	P140	319
I/O	-	-	P99	T4	P109	P141	322
GND	-	-	P100	P6	P110	P142	-
I/O (D1)	P69	P73	P101	T3	P113	P147	325
I/O ($\overline{\text{RCLK}}$, RDY/ $\overline{\text{BUSY}}$)	P70	P74	P102	P5	P114	P148	328
I/O	-	-	P103	R4	P115	P149	331
I/O	-	-	P104	R3	P116	P150	334
I/O (D0, DIN)	P71	P75	P105	P4	P117	P151	337
I/O, SGCK4 (DOUT)	P72	P76	P106	T2	P118	P152	340
CCLK	P73	P77	P107	R2	P119	P153	-
VCC	P74	P78	P108	P3	P120	P154	-
O, TDO	P75	P79	P109	T1	P121	P159	0
GND	P76	P80	P110	N3	P122	P160	-
I/O (A0, $\overline{\text{WS}}$)	P77	P81	P111	R1	P123	P161	2
I/O, PGCK4 (A1)	P78	P82	P112	P2	P124	P162	5
I/O	-	-	P113	N2	P125	P163	8
I/O	-	-	P114	M3	P126	P164	11
I/O (CS1, A2)	P79	P83	P115	P1	P127	P165	14
I/O (A3)	P80	P84	P116	N1	P128	P166	17
GND	-	-	P118	L3	P131	P171	-
I/O	-	-	P119	L2	P132	P172	20
I/O	-	-	P120	L1	P133	P173	23
I/O (A4)	P81	P85	P121	K3	P134	P174	26
I/O (A5)	P82	P86	P122	K2	P135	P175	29
I/O	-	P87	P123	K1	P137	P178	32
I/O	-	P88	P124	J1	P138	P179	35
I/O (A6)	P83	P89	P125	J2	P139	P180	38
I/O (A7)	P84	P90	P126	J3	P140	P181	41
GND	P1	P91	P127	H2	P141	P182	-

4/2/96

Additional No Connect (N.C.) Connections on TQ144, PG156, PQ160 & PQ208 Packages

TQ144	PG156	PQ160	PQ208
P117	A4	P8	P1
	A12	P9	P3
	D1	P30	P10-P13
	D2	P31	P19-P20
	D16	P49	P31-P32
	E15	P50	P38-P41
	M1	P71	P51-P54
	M2	P72	P63-P66
	M15	P89	P72-P73
	N16	P90	P84-P85
	R5	P111	P91-P94
	R12	P112	P102
	T12	P129	P104-P105
		P130	P107
		P136	P115-P118
		P152	P124-P125
		P153	P136-P137
			P143-P146
			P155-P158
			P167-P170
			P176-P177
			P188-P189
			P195-P198
			P206-P208

3/12/96

Pin Locations for XC4006E Devices

XC4006E Pad Name	PC 84	TQ 144	PG 156	PQ 160	PQ 208	Bndry Scan
VCC	P2	P128	H3	P142	P183	-
I/O (A8)	P3	P129	H1	P143	P184	50
I/O (A9)	P4	P130	G1	P144	P185	53
I/O	-	P131	G2	P145	P186	56
I/O	-	P132	G3	P146	P187	59
I/O (A10)	P5	P133	F1	P147	P190	62
I/O (A11)	P6	P134	F2	P148	P191	65
I/O	-	P135	E1	P149	P192	68
I/O	-	P136	E2	P150	P193	71
GND	-	P137	F3	P151	P194	-
I/O	-	-	D1	P152	P197	74
I/O	-	-	D2	P153	P198	77
I/O (A12)	P7	P138	E3	P154	P199	80
I/O (A13)	P8	P139	C1	P155	P200	83
I/O	-	P140	C2	P156	P201	86
I/O	-	P141	D3	P157	P202	89
I/O (A14)	P9	P142	B1	P158	P203	92
I/O, SGCK1 (A15)	P10	P143	B2	P159	P204	95
VCC	P11	P144	C3	P160	P205	-
GND	P12	P1	C4	P1	P2	-
I/O, PGCK1 (A16)	P13	P2	B3	P2	P4	98
I/O (A17)	P14	P3	A1	P3	P5	101
I/O	-	P4	A2	P4	P6	104
I/O	-	P5	C5	P5	P7	107
I/O, TDI	P15	P6	B4	P6	P8	110
I/O, TCK	P16	P7	A3	P7	P9	113
I/O	-	-	A4	P8	P10	116
I/O	-	-	-	P9	P11	119
GND	-	P8	C6	P10	P14	-
I/O	-	P9	B5	P11	P15	122
I/O	-	P10	B6	P12	P16	125
I/O, TMS	P17	P11	A5	P13	P17	128
I/O	P18	P12	C7	P14	P18	131
I/O	-	P13	B7	P15	P21	134
I/O	-	P14	A6	P16	P22	137
I/O	P19	P15	A7	P17	P23	140
I/O	P20	P16	A8	P18	P24	143
GND	P21	P17	C8	P19	P25	-
VCC	P22	P18	B8	P20	P26	-
I/O	P23	P19	C9	P21	P27	146
I/O	P24	P20	B9	P22	P28	149
I/O	-	P21	A9	P23	P29	152
I/O	-	P22	B10	P24	P30	155
I/O	P25	P23	C10	P25	P33	158
I/O	P26	P24	A10	P26	P34	161
I/O	-	P25	A11	P27	P35	164
I/O	-	P26	B11	P28	P36	167
GND	-	P27	C11	P29	P37	-
I/O	-	-	A12	P30	P40	170
I/O	-	-	-	P31	P41	173
I/O	P27	P28	B12	P32	P42	176
I/O	-	P29	A13	P33	P43	179
I/O	-	P30	A14	P34	P44	182
I/O	-	P31	C12	P35	P45	185
I/O	P28	P32	B13	P36	P46	188
I/O, SCGK2	P29	P33	B14	P37	P47	191
O (M1)	P30	P34	A15	P38	P48	194
GND	P31	P35	C13	P39	P49	-
I (M0)	P32	P36	A16	P40	P50	197
VCC	P33	P37	C14	P41	P55	-
I (M2)	P34	P38	B15	P42	P56	198
I/O, PGCK2	P35	P39	B16	P43	P57	199
I/O (HDC)	P36	P40	D14	P44	P58	202
I/O	-	P41	C15	P45	P59	205
I/O	-	P42	D15	P46	P60	208
I/O	-	P43	E14	P47	P61	211
I/O ($\overline{\text{LDC}}$)	P37	P44	C16	P48	P62	214
I/O	-	-	E15	P49	P63	217
I/O	-	-	D16	P50	P64	220
GND	-	P45	F14	P51	P67	-
I/O	-	P46	F15	P52	P68	223
I/O	-	P47	E16	P53	P69	226
I/O	P38	P48	F16	P54	P70	229
I/O	P39	P49	G14	P55	P71	232
I/O	-	P50	G15	P56	P74	235
I/O	-	P51	G16	P57	P75	238
I/O	P40	P52	H16	P58	P76	241
I/O ($\overline{\text{INIT}}$)	P41	P53	H15	P59	P77	244
VCC	P42	P54	H14	P60	P78	-
GND	P43	P55	J14	P61	P79	-
I/O	P44	P56	J15	P62	P80	247
I/O	P45	P57	J16	P63	P81	250
I/O	-	P58	K16	P64	P82	253
I/O	-	P59	K15	P65	P83	256
I/O	P46	P60	K14	P66	P86	259
I/O	P47	P61	L16	P67	P87	262
I/O	-	P62	M16	P68	P88	265
I/O	-	P63	L15	P69	P89	268
GND	-	P64	L14	P70	P90	-
I/O	-	-	N16	P71	P93	271
I/O	-	-	M15	P72	P94	274
I/O	P48	P65	P16	P73	P95	277
I/O	P49	P66	M14	P74	P96	280
I/O	-	P67	N15	P75	P97	283
I/O	-	P68	P15	P76	P98	286
I/O	P50	P69	N14	P77	P99	289
I/O, SGCK3	P51	P70	R16	P78	P100	292
GND	P52	P71	P14	P79	P101	-
DONE	P53	P72	R15	P80	P103	-
VCC	P54	P73	P13	P81	P106	-
$\overline{\text{PROGRAM}}$	P55	P74	R14	P82	P108	-

XC4006E Pad Name	PC 84	TQ 144	PG 156	PQ 160	PQ 208	Bndry Scan
I/O (D7)	P56	P75	T16	P83	P109	295
I/O, PGCK3	P57	P76	T15	P84	P110	298
I/O	-	P77	R13	P85	P111	301
I/O	-	P78	P12	P86	P112	304
I/O (D6)	P58	P79	T14	P87	P113	307
I/O	-	P80	T13	P88	P114	310
I/O	-	-	R12	P89	P115	313
I/O	-	-	T12	P90	P116	316
GND	-	P81	P11	P91	P119	-
I/O	-	P82	R11	P92	P120	319
I/O	-	P83	T11	P93	P121	322
I/O (D5)	P59	P84	T10	P94	P122	325
I/O ($\overline{CS0}$)	P60	P85	P10	P95	P123	328
I/O	-	P86	R10	P96	P126	331
I/O	-	P87	T9	P97	P127	334
I/O (D4)	P61	P88	R9	P98	P128	337
I/O	P62	P89	P9	P99	P129	340
VCC	P63	P90	R8	P100	P130	-
GND	P64	P91	P8	P101	P131	-
I/O (D3)	P65	P92	T8	P102	P132	343
I/O ($\overline{RS}$)	P66	P93	T7	P103	P133	346
I/O	-	P94	T6	P104	P134	349
I/O	-	P95	R7	P105	P135	352
I/O (D2)	P67	P96	P7	P106	P138	355
I/O	P68	P97	T5	P107	P139	358
I/O	-	P98	R6	P108	P140	361
I/O	-	P99	T4	P109	P141	364
GND	-	P100	P6	P110	P142	-
I/O	-	-	R5	P111	P145	367
I/O	-	-	-	P112	P146	370
I/O (D1)	P69	P101	T3	P113	P147	373
I/O ($\overline{RCLK}$, RDY/$\overline{BUSY}$)	P70	P102	P5	P114	P148	376
I/O	-	P103	R4	P115	P149	379
I/O	-	P104	R3	P116	P150	382
I/O (D0, DIN)	P71	P105	P4	P117	P151	385
I/O, SGCK4 (DOUT)	P72	P106	T2	P118	P152	388
CCLK	P73	P107	R2	P119	P153	-
VCC	P74	P108	P3	P120	P154	-
O, TDO	P75	P109	T1	P121	P159	0
GND	P76	P110	N3	P122	P160	-
I/O (A0, $\overline{WS}$)	P77	P111	R1	P123	P161	2
I/O, PGCK4 (A1)	P78	P112	P2	P124	P162	5
I/O	-	P113	N2	P125	P163	8
I/O	-	P114	M3	P126	P164	11
I/O (CS1, A2)	P79	P115	P1	P127	P165	14
I/O (A3)	P80	P116	N1	P128	P166	17
I/O	-	P117	M2	P129	P167	20
I/O	-	-	M1	P130	P168	23
GND	-	P118	L3	P131	P171	-
I/O	-	P119	L2	P132	P172	26
I/O	-	P120	L1	P133	P173	29
I/O (A4)	P81	P121	K3	P134	P174	32
I/O (A5)	P82	P122	K2	P135	P175	35
I/O	-	P123	K1	P137	P178	38
I/O	-	P124	J1	P138	P179	41
I/O (A6)	P83	P125	J2	P139	P180	44
I/O (A7)	P84	P126	J3	P140	P181	47
GND	P1	P127	H2	P141	P182	-

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Additional No Connect (N.C.) Connections on PQ160 & PQ208 Packages

PQ160	PQ208
P136	P1
	P3
	P12-P13
	P19-20
	P31-P32
	P38-P39
	P51-P54
	P65-P66
	P72-P73
	P84-P85
	P91-P92
	P102
	P104-P105
	P107
	P117-P118
	P124-P125
	P136-P137
	P143-P144
	P155-P158
	P169-P170
	P176-P177
	P188-P189
	P195-P196
	P206-P208

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Pin Locations for XC4008E Devices

XC4008E Pad Name	PC 84	PQ 160	PG 191	PQ 208	Bndry Scan
VCC	P2	P142	J4	P183	-
I/O (A8)	P3	P143	J3	P184	56
I/O (A9)	P4	P144	J2	P185	59
I/O	-	P145	J1	P186	62
I/O	-	P146	H1	P187	65
I/O	-	-	H2	P188	68
I/O	-	-	H3	P189	71
I/O (A10)	P5	P147	G1	P190	74
I/O (A11)	P6	P148	G2	P191	77
I/O	-	P149	F1	P192	80
I/O	-	P150	E1	P193	83
GND	-	P151	G3	P194	-
I/O	-	P152	C1	P197	86
I/O	-	P153	E2	P198	89
I/O (A12)	P7	P154	F3	P199	92
I/O (A13)	P8	P155	D2	P200	95
I/O	-	P156	B1	P201	98
I/O	-	P157	E3	P202	101
I/O (A14)	P9	P158	C2	P203	104
I/O, SGCK1 (A15)	P10	P159	B2	P204	107
VCC	P11	P160	D3	P205	-
GND	P12	P1	D4	P2	-
I/O. PGCK1 (A16)	P13	P2	C3	P4	110
I/O (A17)	P14	P3	C4	P5	113
I/O	-	P4	B3	P6	116
I/O	-	P5	C5	P7	119
I/O, TDI	P15	P6	A2	P8	122
I/O, TCK	P16	P7	B4	P9	125
I/O	-	P8	C6	P10	128
I/O	-	P9	A3	P11	131
GND	-	P10	C7	P14	-
I/O	-	P11	A4	P15	134
I/O	-	P12	A5	P16	137
I/O, TMS	P17	P13	B7	P17	140
I/O	P18	P14	A6	P18	143
I/O	-	-	C8	P19	146
I/O	-	-	A7	P20	149
I/O	-	P15	B8	P21	152
I/O	-	P16	A8	P22	155
I/O	P19	P17	B9	P23	158
I/O	P20	P18	C9	P24	161
GND	P21	P19	D9	P25	-
VCC	P22	P20	D10	P26	-
I/O	P23	P21	C10	P27	164
I/O	P24	P22	B10	P28	167
I/O	-	P23	A9	P29	170
I/O	-	P24	A10	P30	173
I/O	-	-	A11	P31	176
I/O	-	-	C11	P32	179
I/O	P25	P25	B11	P33	182
I/O	P26	P26	A12	P34	185
I/O	-	P27	B12	P35	188
I/O	-	P28	A13	P36	191
GND	-	P29	C12	P37	-
I/O	-	P30	A15	P40	194
I/O	-	P31	C13	P41	197
I/O	P27	P32	B14	P42	200
I/O	-	P33	A16	P43	203
I/O	-	P34	B15	P44	206
I/O	-	P35	C14	P45	209
I/O	P28	P36	A17	P46	212
I/O, SCGK2	P29	P37	B16	P47	215
O (M1)	P30	P38	C15	P48	218
GND	P31	P39	D15	P49	-
I (M0)	P32	P40	A18	P50	221
VCC	P33	P41	D16	P55	-
I (M2)	P34	P42	C16	P56	222
I/O, PGCK2	P35	P43	B17	P57	223
I/O (HDC)	P36	P44	E16	P58	226
I/O	-	P45	C17	P59	229
I/O	-	P46	D17	P60	232
I/O	-	P47	B18	P61	235
I/O ($\overline{\text{LDC}}$)	P37	P48	E17	P62	238
I/O	-	P49	F16	P63	241
I/O	-	P50	C18	P64	244
GND	-	P51	G16	P67	-
I/O	-	P52	E18	P68	247
I/O	-	P53	F18	P69	250
I/O	P38	P54	G17	P70	253
I/O	P39	P55	G18	P71	256
I/O	-	-	H16	P72	259
I/O	-	-	H17	P73	262
I/O	-	P56	H18	P74	265
I/O	-	P57	J18	P75	268
I/O	P40	P58	J17	P76	271
I/O ($\overline{\text{INIT}}$)	P41	P59	J16	P77	274
VCC	P42	P60	J15	P78	-
GND	P43	P61	K15	P79	-
I/O	P44	P62	K16	P80	277
I/O	P45	P63	K17	P81	280
I/O	-	P64	K18	P82	283
I/O	-	P65	L18	P83	286
I/O	-	-	L17	P84	289
I/O	-	-	L16	P85	292
I/O	P46	P66	M18	P86	295
I/O	P47	P67	M17	P87	298
I/O	-	P68	N18	P88	301
I/O	-	P69	P18	P89	304
GND	-	P70	M16	P90	-
I/O	-	P71	T18	P93	307
I/O	-	P72	P17	P94	310
I/O	P48	P73	N16	P95	313

XC4008E Pad Name	PC 84	PQ 160	PG 191	PQ 208	Bndry Scan
I/O	P49	P74	T17	P96	316
I/O	-	P75	R17	P97	319
I/O	-	P76	P16	P98	322
I/O	P50	P77	U18	P99	325
I/O, SGCK3	P51	P78	T16	P100	328
GND	P52	P79	R16	P101	-
DONE	P53	P80	U17	P103	-
VCC	P54	P81	R15	P106	-
$\overline{\text{PROGRAM}}$	P55	P82	V18	P108	-
I/O (D7)	P56	P83	T15	P109	331
I/O, PGCK3	P57	P84	U16	P110	334
I/O	-	P85	T14	P111	337
I/O	-	P86	U15	P112	340
I/O (D6)	P58	P87	V17	P113	343
I/O	-	P88	V16	P114	346
I/O	-	P89	T13	P115	349
I/O	-	P90	U14	P116	352
GND	-	P91	T12	P119	-
I/O	-	P92	U13	P120	355
I/O	-	P93	V13	P121	358
I/O (D5)	P59	P94	U12	P122	361
I/O ($\overline{\text{CS0}}$)	P60	P95	V12	P123	364
I/O	-	-	T11	P124	367
I/O	-	-	U11	P125	370
I/O	-	P96	V11	P126	373
I/O	-	P97	V10	P127	376
I/O (D4)	P61	P98	U10	P128	379
I/O	P62	P99	T10	P129	382
VCC	P63	P100	R10	P130	-
GND	P64	P101	R9	P131	-
I/O (D3)	P65	P102	T9	P132	385
I/O ($\overline{\text{RS}}$)	P66	P103	U9	P133	388
I/O	-	P104	V9	P134	391
I/O	-	P105	V8	P135	394
I/O	-	-	U8	P136	397
I/O	-	-	T8	P137	400
I/O (D2)	P67	P106	V7	P138	403
I/O	P68	P107	U7	P139	406
I/O	-	P108	V6	P140	409
I/O	-	P109	U6	P141	412
GND	-	P110	T7	P142	-
I/O	-	P111	U5	P145	415
I/O	-	P112	T6	P146	418
I/O (D1)	P69	P113	V3	P147	421
I/O ($\overline{\text{RCLK}}$, RDY/$\overline{\text{BUSY}}$)	P70	P114	V2	P148	424
I/O	-	P115	U4	P149	427
I/O	-	P116	T5	P150	430
I/O (D0, DIN)	P71	P117	U3	P151	433
I/O, SGCK4 (DOUT)	P72	P118	T4	P152	436
CCLK	P73	P119	V1	P153	-
VCC	P74	P120	R4	P154	-

XC4008E Pad Name	PC 84	PQ 160	PG 191	PQ 208	Bndry Scan
O, TDO	P75	P121	U2	P159	0
GND	P76	P122	R3	P160	-
I/O (A0, $\overline{\text{WS}}$)	P77	P123	T3	P161	2
I/O, PGCK4 (A1)	P78	P124	U1	P162	5
I/O	-	P125	P3	P163	8
I/O	-	P126	R2	P164	11
I/O (CS1, A2)	P79	P127	T2	P165	14
I/O (A3)	P80	P128	N3	P166	17
I/O	-	P129	P2	P167	20
I/O	-	P130	T1	P168	23
GND	-	P131	M3	P171	-
I/O	-	P132	P1	P172	26
I/O	-	P133	N1	P173	29
I/O (A4)	P81	P134	M2	P174	32
I/O (A5)	P82	P135	M1	P175	35
I/O	-	-	L3	P176	38
I/O	-	P136	L2	P177	41
I/O	-	P137	L1	P178	44
I/O	-	P138	K1	P179	47
I/O (A6)	P83	P139	K2	P180	50
I/O (A7)	P84	P140	K3	P181	53
GND	P1	P141	K4	P182	-

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Additional No Connect (N.C.) Connections on PG191 & PQ208 Packages

PG191	PQ208	PQ208
A14	P1	P107
B5	P3	P117
B6	P12	P118
B13	P13	P143
D1	P38	P144
D18	P39	P155
F2	P51	P156
F17	P52	P157
N2	P53	P158
N17	P54	P169
R1	P65	P170
R18	P66	P195
V4	P91	P196
V5	P92	P206
V14	P102	P207
V15	P104	P208
	P105	

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Pin Locations for XC4010E/L Devices

XC4010E/L Pad Name	PC 84	PQ 160	TQ 176	PG 191	PQ/ HQ 208	BG 225	Bndry Scan
VCC	P2	P142	P155	J4	P183	D8	-
I/O (A8)	P3	P143	P156	J3	P184	E8	62
I/O (A9)	P4	P144	P157	J2	P185	B7	65
I/O	-	P145	P158	J1	P186	A7	68
I/O	-	P146	P159	H1	P187	C7	71
I/O	-	-	P160	H2	P188	D7	74
I/O	-	-	P161	H3	P189	E7	77
I/O (A10)	P5	P147	P162	G1	P190	A6	80
I/O (A11)	P6	P148	P163	G2	P191	B6	83
I/O	-	P149	P164	F1	P192	A5	86
I/O	-	P150	P165	E1	P193	B5	89
GND	-	P151	P166	G3	P194	GND*	-
I/O	-	-	-	F2	P195	D6	92
I/O	-	-	P167	D1	P196	C5	95
I/O	-	P152	P168	C1	P197	A4	98
I/O	-	P153	P169	E2	P198	E6	101
I/O (A12)	P7	P154	P170	F3	P199	B4	104
I/O (A13)	P8	P155	P171	D2	P200	D5	107
I/O	-	P156	P172	B1	P201	B3	110
I/O	-	P157	P173	E3	P202	F6	113
I/O (A14)	P9	P158	P174	C2	P203	A2	116
I/O, SGCK1 (A15)	P10	P159	P175	B2	P204	C3	119
VCC	P11	P160	P176	D3	P205	B2	-
GND	P12	P1	P1	D4	P2	A1	-
I/O, PGCK1 (A16)	P13	P2	P2	C3	P4	D4	122
I/O (A17)	P14	P3	P3	C4	P5	B1	125
I/O	-	P4	P4	B3	P6	C2	128
I/O	-	P5	P5	C5	P7	E5	131
I/O, TDI	P15	P6	P6	A2	P8	D3	134
I/O, TCK	P16	P7	P7	B4	P9	C1	137
I/O	-	P8	P8	C6	P10	D2	140
I/O	-	P9	P9	A3	P11	G6	143
I/O	-	-	-	B5	P12	E4	146
I/O	-	-	-	B6	P13	D1	149
GND	-	P10	P10	C7	P14	GND*	-
I/O	-	P11	P11	A4	P15	F5	152
I/O	-	P12	P12	A5	P16	E1	155
I/O, TMS	P17	P13	P13	B7	P17	F4	158
I/O	P18	P14	P14	A6	P18	F3	161
I/O	-	-	P15	C8	P19	G4	164
I/O	-	-	P16	A7	P20	G3	167
I/O	-	P15	P17	B8	P21	G2	170
I/O	-	P16	P18	A8	P22	G1	173
I/O	P19	P17	P19	B9	P23	G5	176
I/O	P20	P18	P20	C9	P24	H3	179
GND	P21	P19	P21	D9	P25	H2	-
VCC	P22	P20	P22	D10	P26	H1	-
I/O	P23	P21	P23	C10	P27	H4	182
I/O	P24	P22	P24	B10	P28	H5	185
I/O	-	P23	P25	A9	P29	J2	188
I/O	-	P24	P26	A10	P30	J1	191
I/O	-	-	P27	A11	P31	J3	194
I/O	-	-	P28	C11	P32	J4	197
I/O	P25	P25	P29	B11	P33	K2	200
I/O	P26	P26	P30	A12	P34	K3	203
I/O	-	P27	P31	B12	P35	J6	206
I/O	-	P28	P32	A13	P36	L1	209
GND	-	P29	P33	C12	P37	GND*	-
I/O	-	-	-	B13	P38	L3	212
I/O	-	-	-	A14	P39	M1	215
I/O	-	P30	P34	A15	P40	K5	218
I/O	-	P31	P35	C13	P41	M2	221
I/O	P27	P32	P36	B14	P42	L4	224
I/O	-	P33	P37	A16	P43	N1	227
I/O	-	P34	P38	B15	P44	M3	230
I/O	-	P35	P39	C14	P45	N2	233
I/O	P28	P36	P40	A17	P46	K6	236
I/O, SCGK2	P29	P37	P41	B16	P47	P1	239
O (M1)	P30	P38	P42	C15	P48	N3	242
GND	P31	P39	P43	D15	P49	GND*	-
I (M0)	P32	P40	P44	A18	P50	P2	245
VCC	P33	P41	P45	D16	P55	R1	-
I (M2)	P34	P42	P46	C16	P56	M4	246
I/O, PGCK2	P35	P43	P47	B17	P57	R2	247
I/O (HDC)	P36	P44	P48	E16	P58	P3	250
I/O	-	P45	P49	C17	P59	L5	253
I/O	-	P46	P50	D17	P60	N4	256
I/O	-	P47	P51	B18	P61	R3	259
I/O ($\overline{\text{LDC}}$)	P37	P48	P52	E17	P62	P4	262
I/O	-	P49	P53	F16	P63	K7	265
I/O	-	P50	P54	C18	P64	M5	268
I/O	-	-	-	D18	P65	R4	271
I/O	-	-	-	F17	P66	N5	274
GND	-	P51	P55	G16	P67	GND*	-
I/O	-	P52	P56	E18	P68	R5	277
I/O	-	P53	P57	F18	P69	M6	280
I/O	P38	P54	P58	G17	P70	N6	283
I/O	P39	P55	P59	G18	P71	P6	286
I/O	-	-	P60	H16	P72	R6	289

XC4010E/L Pad Name	PC 84	PQ 160	TQ 176	PG 191	PQ/ HQ 208	BG 225	Bndry Scan
I/O	-	-	P61	H17	P73	M7	292
I/O	-	P56	P62	H18	P74	R7	295
I/O	-	P57	P63	J18	P75	L7	298
I/O	P40	P58	P64	J17	P76	N8	301
I/O ($\overline{INIT}$)	P41	P59	P65	J16	P77	P8	304
VCC	P42	P60	P66	J15	P78	R8	-
GND	P43	P61	P67	K15	P79	M8	-
I/O	P44	P62	P68	K16	P80	L8	307
I/O	P45	P63	P69	K17	P81	P9	310
I/O	-	P64	P70	K18	P82	R9	313
I/O	-	P65	P71	L18	P83	N9	316
I/O	-	-	P72	L17	P84	M9	319
I/O	-	-	P73	L16	P85	L9	322
I/O	P46	P66	P74	M18	P86	N10	325
I/O	P47	P67	P75	M17	P87	K9	328
I/O	-	P68	P76	N18	P88	R11	331
I/O	-	P69	P77	P18	P89	P11	334
GND	-	P70	P78	M16	P90	GND*	-
I/O	-	-	-	N17	P91	R12	337
I/O	-	-	-	R18	P92	L10	340
I/O	-	P71	P79	T18	P93	P12	343
I/O	-	P72	P80	P17	P94	M11	346
I/O	P48	P73	P81	N16	P95	R13	349
I/O	P49	P74	P82	T17	P96	N12	352
I/O	-	P75	P83	R17	P97	P13	355
I/O	-	P76	P84	P16	P98	K10	358
I/O	P50	P77	P85	U18	P99	R14	361
I/O, SGCK3	P51	P78	P86	T16	P100	N13	364
GND	P52	P79	P87	R16	P101	GND*	-
DONE	P53	P80	P88	U17	P103	P14	-
VCC	P54	P81	P89	R15	P106	R15	-
$\overline{PROGRAM}$	P55	P82	P90	V18	P108	M12	-
I/O (D7)	P56	P83	P91	T15	P109	P15	367
I/O, PGCK3	P57	P84	P92	U16	P110	N14	370
I/O	-	P85	P93	T14	P111	L11	373
I/O	-	P86	P94	U15	P112	M13	376
I/O (D6)	P58	P87	P95	V17	P113	J10	379
I/O	-	P88	P96	V16	P114	L12	382
I/O	-	P89	P97	T13	P115	M15	385
I/O	-	P90	P98	U14	P116	L13	388
I/O	-	-	-	V15	P117	L14	391
I/O	-	-	-	V14	P118	K11	394
GND	-	P91	P99	T12	P119	GND*	-
I/O	-	P92	P100	U13	P120	K13	397
I/O	-	P93	P101	V13	P121	K14	400
I/O (D5)	P59	P94	P102	U12	P122	K15	403

XC4010E/L Pad Name	PC 84	PQ 160	TQ 176	PG 191	PQ/ HQ 208	BG 225	Bndry Scan
I/O ($\overline{CS0}$)	P60	P95	P103	V12	P123	J12	406
I/O	-	-	P104	T11	P124	J13	409
I/O	-	-	P105	U11	P125	J14	412
I/O	-	P96	P106	V11	P126	J15	415
I/O	-	P97	P107	V10	P127	J11	418
I/O (D4)	P61	P98	P108	U10	P128	H13	421
I/O	P62	P99	P109	T10	P129	H14	424
VCC	P63	P100	P110	R10	P130	H15	-
GND	P64	P101	P111	R9	P131	GND*	-
I/O (D3)	P65	P102	P112	T9	P132	H12	427
I/O ($\overline{RS}$)	P66	P103	P113	U9	P133	H11	430
I/O	-	P104	P114	V9	P134	G14	433
I/O	-	P105	P115	V8	P135	G15	436
I/O	-	-	P116	U8	P136	G13	439
I/O	-	-	P117	T8	P137	G12	442
I/O (D2)	P67	P106	P118	V7	P138	G11	445
I/O	P68	P107	P119	U7	P139	F15	448
I/O	-	P108	P120	V6	P140	F14	451
I/O	-	P109	P121	U6	P141	F13	454
GND	-	P110	P122	T7	P142	GND*	-
I/O	-	-	-	V5	P143	E13	457
I/O	-	-	-	V4	P144	D15	460
I/O	-	P111	P123	U5	P145	F11	463
I/O	-	P112	P124	T6	P146	D14	466
I/O (D1)	P69	P113	P125	V3	P147	E12	469
I/O ($\overline{RCLK}$, $\overline{RDY}$/ $\overline{BUSY}$)	P70	P114	P126	V2	P148	C15	472
I/O	-	P115	P127	U4	P149	D13	475
I/O	-	P116	P128	T5	P150	C14	478
I/O (D0, DIN)	P71	P117	P129	U3	P151	F10	481
I/O, SGCK4 (DOUT)	P72	P118	P130	T4	P152	B15	484
CCLK	P73	P119	P131	V1	P153	C13	-
VCC	P74	P120	P132	R4	P154	B14	-
O, TDO	P75	P121	P133	U2	P159	A15	0
GND	P76	P122	P134	R3	P160	D12	-
I/O (A0, $\overline{WS}$)	P77	P123	P135	T3	P161	A14	2
I/O, PGCK4 (A1)	P78	P124	P136	U1	P162	B13	5
I/O	-	P125	P137	P3	P163	E11	8
I/O	-	P126	P138	R2	P164	C12	11
I/O (CS1, A2)	P79	P127	P139	T2	P165	A13	14
I/O (A3)	P80	P128	P140	N3	P166	B12	17

XC4010E/L Pad Name	PC 84	PQ 160	TQ 176	PG 191	PQ/ HQ 208	BG 225	Bndry Scan
I/O	-	P129	P141	P2	P167	A12	20
I/O	-	P130	P142	T1	P168	C11	23
I/O	-	-	-	R1	P169	B11	26
I/O	-	-	-	N2	P170	E10	29
GND	-	P131	P143	M3	P171	GND*	-
I/O	-	P132	P144	P1	P172	A11	32
I/O	-	P133	P145	N1	P173	D10	35
I/O (A4)	P81	P134	P146	M2	P174	A10	38
I/O (A5)	P82	P135	P147	M1	P175	D9	41
I/O	-	-	P148	L3	P176	C9	44
I/O	-	P136	P149	L2	P177	B9	47
I/O	-	P137	P150	L1	P178	A9	50
I/O	-	P138	P151	K1	P179	E9	53
I/O (A6)	P83	P139	P152	K2	P180	C8	56
I/O (A7)	P84	P140	P153	K3	P181	B8	59
GND	P1	P141	P154	K4	P182	A8	-

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* Pads labelled GND* are internally bonded to a Ground plane within the BG225 package. They have no direct connection to any package pin.

Additional Ground (GND) Connections on BG225 Package

GND
F8
G7
G8
G9
H6
H7
H8
H9
H10
J7
J8
J9
K8

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Note: The package pins in this table are bonded to an internal Ground plane within the BG225 package. They should all be externally connected to Ground.

Additional No Connect (N.C.) Connections on PQ/ HQ208 & BG225 Packages

PQ/HQ208	BG225
P1	A3
P3	B10
P51	C4
P52	C6
P53	C10
P54	D11
P102	E2
P104	E3
P105	E14
P107	E15
P155	F1
P156	F2
P157	F7
P158	F9
P206	F12
P207	G10
P208	J5
	K1
	K4
	K12
	L2
	L6
	L15
	M10
	M14
	N7
	N11
	N15
	P5
	P7
	P10
	R10

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Pin Locations for XC4013E/L Devices

XC4013E/L Pad Name	PQ 160	PQ/ HQ 208	PG 223	BG 225	PQ/ HQ 240	Bndry Scan
VCC	P142	P183	J4	D8	P212	-
I/O (A8)	P143	P184	J3	E8	P213	74
I/O (A9)	P144	P185	J2	B7	P214	77
I/O	P145	P186	J1	A7	P215	80
I/O	P146	P187	H1	C7	P216	83
I/O	-	P188	H2	D7	P217	86
I/O	-	P189	H3	E7	P218	89
I/O (A10)	P147	P190	G1	A6	P220	92
I/O (A11)	P148	P191	G2	B6	P221	95
VCC	-	-	-	VCC*	P222	-
I/O	-	-	H4	C6	P223	98
I/O	-	-	G4	F7	P224	101
I/O	P149	P192	F1	A5	P225	104
I/O	P150	P193	E1	B5	P226	107
GND	P151	P194	G3	GND*	P227	-
I/O	-	P195	F2	D6	P228	110
I/O	-	P196	D1	C5	P229	113
I/O	P152	P197	C1	A4	P230	116
I/O	P153	P198	E2	E6	P231	119
I/O (A12)	P154	P199	F3	B4	P232	122
I/O (A13)	P155	P200	D2	D5	P233	125
I/O	-	-	F4	A3	P234	128
I/O	-	-	E4	C4	P235	131
I/O	P156	P201	B1	B3	P236	134
I/O	P157	P202	E3	F6	P237	137
I/O (A14)	P158	P203	C2	A2	P238	140
I/O, SGCK1 (A15)	P159	P204	B2	C3	P239	143
VCC	P160	P205	D3	B2	P240	-
GND	P1	P2	D4	A1	P1	-
I/O, PGCK1 (A16)	P2	P4	C3	D4	P2	146
I/O (A17)	P3	P5	C4	B1	P3	149
I/O	P4	P6	B3	C2	P4	152
I/O	P5	P7	C5	E5	P5	155
I/O, TDI	P6	P8	A2	D3	P6	158
I/O, TCK	P7	P9	B4	C1	P7	161
I/O	P8	P10	C6	D2	P8	164
I/O	P9	P11	A3	G6	P9	167
I/O	-	P12	B5	E4	P10	170
I/O	-	P13	B6	D1	P11	173
I/O	-	-	D5	E3	P12	176
I/O	-	-	D6	E2	P13	179
GND	P10	P14	C7	GND*	P14	-
I/O	P11	P15	A4	F5	P15	182
I/O	P12	P16	A5	E1	P16	185
I/O, TMS	P13	P17	B7	F4	P17	188
I/O	P14	P18	A6	F3	P18	191
VCC	-	-	-	VCC*	P19	-
I/O	-	-	D7	F2	P20	194
I/O	-	-	D8	F1	P21	197
I/O	-	P19	C8	G4	P23	200
I/O	-	P20	A7	G3	P24	203
I/O	P15	P21	B8	G2	P25	206
I/O	P16	P22	A8	G1	P26	209
I/O	P17	P23	B9	G5	P27	212
I/O	P18	P24	C9	H3	P28	215
GND	P19	P25	D9	H2	P29	-
VCC	P20	P26	D10	H1	P30	-
I/O	P21	P27	C10	H4	P31	218
I/O	P22	P28	B10	H5	P32	221
I/O	P23	P29	A9	J2	P33	224
I/O	P24	P30	A10	J1	P34	227
I/O	-	P31	A11	J3	P35	230
I/O	-	P32	C11	J4	P36	233
I/O	-	-	D11	J5	P38	236
I/O	-	-	D12	K1	P39	239
VCC	-	-	-	VCC*	P40	-
I/O	P25	P33	B11	K2	P41	242
I/O	P26	P34	A12	K3	P42	245
I/O	P27	P35	B12	J6	P43	248
I/O	P28	P36	A13	L1	P44	251
GND	P29	P37	C12	GND*	P45	-
I/O	-	-	D13	L2	P46	254
I/O	-	-	D14	K4	P47	257
I/O	-	P38	B13	L3	P48	260
I/O	-	P39	A14	M1	P49	263
I/O	P30	P40	A15	K5	P50	266
I/O	P31	P41	C13	M2	P51	269
I/O	P32	P42	B14	L4	P52	272
I/O	P33	P43	A16	N1	P53	275
I/O	P34	P44	B15	M3	P54	278
I/O	P35	P45	C14	N2	P55	281
I/O	P36	P46	A17	K6	P56	284
I/O, SCGK2	P37	P47	B16	P1	P57	287
O (M1)	P38	P48	C15	N3	P58	290
GND	P39	P49	D15	GND*	P59	-
I (M0)	P40	P50	A18	P2	P60	293
VCC	P41	P55	D16	R1	P61	-
I (M2)	P42	P56	C16	M4	P62	294
I/O, PGCK2	P43	P57	B17	R2	P63	295
I/O (HDC)	P44	P58	E16	P3	P64	298
I/O	P45	P59	C17	L5	P65	301
I/O	P46	P60	D17	N4	P66	304
I/O	P47	P61	B18	R3	P67	307
I/O (LDC)	P48	P62	E17	P4	P68	310
I/O	P49	P63	F16	K7	P69	313
I/O	P50	P64	C18	M5	P70	316
I/O	-	P65	D18	R4	P71	319

XC4013E/L Pad Name	PQ 160	PQ/ HQ 208	PG 223	BG 225	PQ/ HQ 240	Bndry Scan
I/O	-	P66	F17	N5	P72	322
I/O	-	-	E15	P5	P73	325
I/O	-	-	F15	L6	P74	328
GND	P51	P67	G16	GND*	P75	-
I/O	P52	P68	E18	R5	P76	331
I/O	P53	P69	F18	M6	P77	334
I/O	P54	P70	G17	N6	P78	337
I/O	P55	P71	G18	P6	P79	340
VCC	-	-	-	VCC*	P80	-
I/O	-	P72	H16	R6	P81	343
I/O	-	P73	H17	M7	P82	346
I/O	-	-	G15	N7	P84	349
I/O	-	-	H15	P7	P85	352
I/O	P56	P74	H18	R7	P86	355
I/O	P57	P75	J18	L7	P87	358
I/O	P58	P76	J17	N8	P88	361
I/O ($\overline{INIT}$)	P59	P77	J16	P8	P89	364
VCC	P60	P78	J15	R8	P90	-
GND	P61	P79	K15	M8	P91	-
I/O	P62	P80	K16	L8	P92	367
I/O	P63	P81	K17	P9	P93	370
I/O	P64	P82	K18	R9	P94	373
I/O	P65	P83	L18	N9	P95	376
I/O	-	P84	L17	M9	P96	379
I/O	-	P85	L16	L9	P97	382
I/O	-	-	L15	R10	P99	385
I/O	-	-	M15	P10	P100	388
VCC	-	-	-	VCC*	P101	-
I/O	P66	P86	M18	N10	P102	391
I/O	P67	P87	M17	K9	P103	394
I/O	P68	P88	N18	R11	P104	397
I/O	P69	P89	P18	P11	P105	400
GND	P70	P90	M16	GND*	P106	-
I/O	-	-	N15	M10	P107	403
I/O	-	-	P15	N11	P108	406
I/O	-	P91	N17	R12	P109	409
I/O	-	P92	R18	L10	P110	412
I/O	P71	P93	T18	P12	P111	415
I/O	P72	P94	P17	M11	P112	418
I/O	P73	P95	N16	R13	P113	421
I/O	P74	P96	T17	N12	P114	424
I/O	P75	P97	R17	P13	P115	427
I/O	P76	P98	P16	K10	P116	430
I/O	P77	P99	U18	R14	P117	433
I/O, SGCK3	P78	P100	T16	N13	P118	436
GND	P79	P101	R16	GND*	P119	-
DONE	P80	P103	U17	P14	P120	-
VCC	P81	P106	R15	R15	P121	-
$\overline{PROGRAM}$	P82	P108	V18	M12	P122	-
I/O (D7)	P83	P109	T15	P15	P123	439

XC4013E/L Pad Name	PQ 160	PQ/ HQ 208	PG 223	BG 225	PQ/ HQ 240	Bndry Scan
I/O, PGCK3	P84	P110	U16	N14	P124	442
I/O	P85	P111	T14	L11	P125	445
I/O	P86	P112	U15	M13	P126	448
I/O	-	-	R14	N15	P127	451
I/O	-	-	R13	M14	P128	454
I/O (D6)	P87	P113	V17	J10	P129	457
I/O	P88	P114	V16	L12	P130	460
I/O	P89	P115	T13	M15	P131	463
I/O	P90	P116	U14	L13	P132	466
I/O	-	P117	V15	L14	P133	469
I/O	-	P118	V14	K11	P134	472
GND	P91	P119	T12	GND*	P135	-
I/O	-	-	R12	L15	P136	475
I/O	-	-	R11	K12	P137	478
I/O	P92	P120	U13	K13	P138	481
I/O	P93	P121	V13	K14	P139	484
VCC	-	-	-	VCC*	P140	-
I/O (D5)	P94	P122	U12	K15	P141	487
I/O ($\overline{CS0}$)	P95	P123	V12	J12	P142	490
I/O	-	P124	T11	J13	P144	493
I/O	-	P125	U11	J14	P145	496
I/O	P96	P126	V11	J15	P146	499
I/O	P97	P127	V10	J11	P147	502
I/O (D4)	P98	P128	U10	H13	P148	505
I/O	P99	P129	T10	H14	P149	508
VCC	P100	P130	R10	H15	P150	-
GND	P101	P131	R9	GND*	P151	-
I/O (D3)	P102	P132	T9	H12	P152	511
I/O ($\overline{RS}$)	P103	P133	U9	H11	P153	514
I/O	P104	P134	V9	G14	P154	517
I/O	P105	P135	V8	G15	P155	520
I/O	-	P136	U8	G13	P156	523
I/O	-	P137	T8	G12	P157	526
I/O (D2)	P106	P138	V7	G11	P159	529
I/O	P107	P139	U7	F15	P160	532
VCC	-	-	-	VCC*	P161	-
I/O	P108	P140	V6	F14	P162	535
I/O	P109	P141	U6	F13	P163	538
I/O	-	-	R8	G10	P164	541
I/O	-	-	R7	E15	P165	544
GND	P110	P142	T7	GND*	P166	-
I/O	-	-	R6	E14	P167	547
I/O	-	-	R5	F12	P168	550
I/O	-	P143	V5	E13	P169	553
I/O	-	P144	V4	D15	P170	556
I/O	P111	P145	U5	F11	P171	559
I/O	P112	P146	T6	D14	P172	562
I/O (D1)	P113	P147	V3	E12	P173	565
I/O ($\overline{RCLK}$, RDY/$\overline{BUSY}$)	P114	P148	V2	C15	P174	568
I/O	P115	P149	U4	D13	P175	571

XC4013E/L Pad Name	PQ 160	PQ/ HQ 208	PG 223	BG 225	PQ/ HQ 240	Bndry Scan
I/O	P116	P150	T5	C14	P176	574
I/O (D0, DIN)	P117	P151	U3	F10	P177	577
I/O, SGCK4 (DOUT)	P118	P152	T4	B15	P178	580
CCLK	P119	P153	V1	C13	P179	-
VCC	P120	P154	R4	B14	P180	-
O, TDO	P121	P159	U2	A15	P181	0
GND	P122	P160	R3	D12	P182	-
I/O (A0, $\overline{WS}$)	P123	P161	T3	A14	P183	2
I/O, PGCK4 (A1)	P124	P162	U1	B13	P184	5
I/O	P125	P163	P3	E11	P185	8
I/O	P126	P164	R2	C12	P186	11
I/O (CS1, A2)	P127	P165	T2	A13	P187	14
I/O (A3)	P128	P166	N3	B12	P188	17
I/O	-	-	P4	F9	P189	20
I/O	-	-	N4	D11	P190	23
I/O	P129	P167	P2	A12	P191	26
I/O	P130	P168	T1	C11	P192	29
I/O	-	P169	R1	B11	P193	32
I/O	-	P170	N2	E10	P194	35
GND	P131	P171	M3	GND*	P196	-
I/O	P132	P172	P1	A11	P197	38
I/O	P133	P173	N1	D10	P198	41
I/O	-	-	M4	C10	P199	44
I/O	-	-	L4	B10	P200	47
VCC	-	-	-	VCC*	P201	-
I/O (A4)	P134	P174	M2	A10	P202	50
I/O (A5)	P135	P175	M1	D9	P203	53
I/O	-	P176	L3	C9	P205	56
I/O	P136	P177	L2	B9	P206	59
I/O	P137	P178	L1	A9	P207	62
I/O	P138	P179	K1	E9	P208	65
I/O (A6)	P139	P180	K2	C8	P209	68
I/O (A7)	P140	P181	K3	B8	P210	71
GND	P141	P182	K4	A8	P211	-

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Pads labelled GND* are internally bonded to a Ground plane within the BG225 package. They have no direct connection to any package pin.

Pads labelled VCC* are internally bonded to a Vcc plane within the BG225 package. They have no direct connection to any package pin.

Additional Ground (GND) Connections on BG225 Packages

BG225	BG225
K8	H9
J7	H10
J8	G7
J9	G8
H6	G9
H7	F8
H8	

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The BG225 package pins in this table are bonded to an internal Ground plane on the XC4013E/L die. They must all be externally connected to Ground.

Additional No Connect (N.C.) Connections on PQ/HQ208 & PQ/HQ240 Packages

PQ/HQ208	PQ/HQ240
P1	P22 ‡
P3	P37 ‡
P51	P83 ‡
P52	P98 ‡
P53	P143 ‡
P54	P158 ‡
P102	P195
P104	P204 ‡
P105	P219 ‡
P107	
P155	
P156	
P157	
P158	
P206	
P207	
P208	

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‡ Pins marked with this symbol are reserved for Ground connections on future revisions of the device. These pins do not physically connect to anything on the current device revision. However, they should be externally connected to Ground, if possible.

Pin Locations for XC4020E Devices

XC4020E Pad Name	HQ 208	PG 223	HQ 240	Bndry Scan
VCC	P183	J4	P212	-
I/O (A8)	P184	J3	P213	86
I/O (A9)	P185	J2	P214	89
I/O	P186	J1	P215	92
I/O	P187	H1	P216	95
I/O	P188	H2	P217	98
I/O	P189	H3	P218	101
I/O (A10)	P190	G1	P220	104
I/O (A11)	P191	G2	P221	107
I/O	-	-	-	110
I/O	-	-	-	113
VCC	-	-	P222	-
I/O	-	H4	P223	116
I/O	-	G4	P224	119
I/O	P192	F1	P225	122
I/O	P193	E1	P226	125
GND	P194	G3	P227	-
I/O	P195	F2	P228	128
I/O	P196	D1	P229	131
I/O	P197	C1	P230	134
I/O	P198	E2	P231	137
I/O (A12)	P199	F3	P232	140
I/O (A13)	P200	D2	P233	143
I/O	-	-	-	146
I/O	-	-	-	149
I/O	-	F4	P234	152
I/O	-	E4	P235	155
I/O	P201	B1	P236	158
I/O	P202	E3	P237	161
I/O (A14)	P203	C2	P238	164
I/O, SGCK1 (A15)	P204	B2	P239	167
VCC	P205	D3	P240	-
GND	P2	D4	P1	-
I/O, PGCK1 (A16)	P4	C3	P2	170
I/O (A17)	P5	C4	P3	173
I/O	P6	B3	P4	176
I/O	P7	C5	P5	179
I/O, TDI	P8	A2	P6	182
I/O, TCK	P9	B4	P7	185
I/O	-	-	-	188
I/O	-	-	-	191
I/O	P10	C6	P8	194
I/O	P11	A3	P9	197
I/O	P12	B5	P10	200
I/O	P13	B6	P11	203
I/O	-	D5	P12	206
I/O	-	D6	P13	209
GND	P14	C7	P14	-
I/O	P15	A4	P15	212
I/O	P16	A5	P16	215
I/O, TMS	P17	B7	P17	218
I/O	P18	A6	P18	221
VCC	-	-	P19	-
I/O	-	D7	P20	224
I/O	-	D8	P21	227
I/O	-	-	-	230
I/O	-	-	-	233
I/O	P19	C8	P23	236
I/O	P20	A7	P24	239
I/O	P21	B8	P25	242
I/O	P22	A8	P26	245
I/O	P23	B9	P27	248
I/O	P24	C9	P28	251
GND	P25	D9	P29	-
VCC	P26	D10	P30	-
I/O	P27	C10	P31	254
I/O	P28	B10	P32	257
I/O	P29	A9	P33	260
I/O	P30	A10	P34	263
I/O	P31	A11	P35	266
I/O	P32	C11	P36	269
I/O	-	-	-	272
I/O	-	-	-	275
I/O	-	D11	P38	278
I/O	-	D12	P39	281
VCC	-	-	P40	-
I/O	P33	B11	P41	284
I/O	P34	A12	P42	287
I/O	P35	B12	P43	290
I/O	P36	A13	P44	293
GND	P37	C12	P45	-
I/O	-	D13	P46	296
I/O	-	D14	P47	299
I/O	P38	B13	P48	302
I/O	P39	A14	P49	305
I/O	P40	A15	P50	308
I/O	P41	C13	P51	311
I/O	-	-	-	314
I/O	-	-	-	317
I/O	P42	B14	P52	320
I/O	P43	A16	P53	323
I/O	P44	B15	P54	326
I/O	P45	C14	P55	329
I/O	P46	A17	P56	332
I/O, SCGK2	P47	B16	P57	335
O (M1)	P48	C15	P58	338
GND	P49	D15	P59	-
I (M0)	P50	A18	P60	341
VCC	P55	D16	P61	-
I (M2)	P56	C16	P62	342
I/O, PGCK2	P57	B17	P63	343
I/O (HDC)	P58	E16	P64	346

XC4020E Pad Name	HQ 208	PG 223	HQ 240	Bndry Scan
I/O	P59	C17	P65	349
I/O	P60	D17	P66	352
I/O	P61	B18	P67	355
I/O ($\overline{LDC}$)	P62	E17	P68	358
I/O	-	-	-	361
I/O	-	-	-	364
I/O	P63	F16	P69	367
I/O	P64	C18	P70	370
I/O	P65	D18	P71	373
I/O	P66	F17	P72	376
I/O	-	E15	P73	379
I/O	-	F15	P74	382
GND	P67	G16	P75	-
I/O	P68	E18	P76	385
I/O	P69	F18	P77	388
I/O	P70	G17	P78	391
I/O	P71	G18	P79	394
VCC	-	-	P80	-
I/O	P72	H16	P81	397
I/O	P73	H17	P82	400
I/O	-	-	-	403
I/O	-	-	-	406
I/O	-	G15	P84	409
I/O	-	H15	P85	412
I/O	P74	H18	P86	415
I/O	P75	J18	P87	418
I/O	P76	J17	P88	421
I/O ($\overline{INIT}$)	P77	J16	P89	424
VCC	P78	J15	P90	-
GND	P79	K15	P91	-
I/O	P80	K16	P92	427
I/O	P81	K17	P93	430
I/O	P82	K18	P94	433
I/O	P83	L18	P95	436
I/O	P84	L17	P96	439
I/O	P85	L16	P97	442
I/O	-	-	-	445
I/O	-	-	-	448
I/O	-	L15	P99	451
I/O	-	M15	P100	454
VCC	-	-	P101	-
I/O	P86	M18	P102	457
I/O	P87	M17	P103	460
I/O	P88	N18	P104	463
I/O	P89	P18	P105	466
GND	P90	M16	P106	-
I/O	-	N15	P107	469
I/O	-	P15	P108	472
I/O	P91	N17	P109	475
I/O	P92	R18	P110	478
I/O	P93	T18	P111	481
I/O	P94	P17	P112	484

XC4020E Pad Name	HQ 208	PG 223	HQ 240	Bndry Scan
I/O	-	-	-	487
I/O	-	-	-	490
I/O	P95	N16	P113	493
I/O	P96	T17	P114	496
I/O	P97	R17	P115	499
I/O	P98	P16	P116	502
I/O	P99	U18	P117	505
I/O, SGCK3	P100	T16	P118	508
GND	P101	R16	P119	-
DONE	P103	U17	P120	-
VCC	P106	R15	P121	-
$\overline{PROGRAM}$	P108	V18	P122	-
I/O (D7)	P109	T15	P123	511
I/O, PGCK3	P110	U16	P124	514
I/O	P111	T14	P125	517
I/O	P112	U15	P126	520
I/O	-	R14	P127	523
I/O	-	R13	P128	526
I/O	-	-	-	529
I/O	-	-	-	532
I/O (D6)	P113	V17	P129	535
I/O	P114	V16	P130	538
I/O	P115	T13	P131	541
I/O	P116	U14	P132	544
I/O	P117	V15	P133	547
I/O	P118	V14	P134	550
GND	P119	T12	P135	-
I/O	-	R12	P136	553
I/O	-	R11	P137	556
I/O	P120	U13	P138	559
I/O	P121	V13	P139	562
VCC	-	-	P140	-
I/O (D5)	P122	U12	P141	565
I/O ($\overline{CS0}$)	P123	V12	P142	568
I/O	-	-	-	571
I/O	-	-	-	574
I/O	P124	T11	P144	577
I/O	P125	U11	P145	580
I/O	P126	V11	P146	583
I/O	P127	V10	P147	586
I/O (D4)	P128	U10	P148	589
I/O	P129	T10	P149	592
VCC	P130	R10	P150	-
GND	P131	R9	P151	-
I/O (D3)	P132	T9	P152	595
I/O ($\overline{RS}$)	P133	U9	P153	598
I/O	P134	V9	P154	601
I/O	P135	V8	P155	604
I/O	P136	U8	P156	607
I/O	P137	T8	P157	610
I/O	-	-	-	613
I/O	-	-	-	616

XC4020E Pad Name	HQ 208	PG 223	HQ 240	Bndry Scan
I/O (D2)	P138	V7	P159	619
I/O	P139	U7	P160	622
VCC	-	-	P161	-
I/O	P140	V6	P162	625
I/O	P141	U6	P163	628
I/O	-	R8	P164	631
I/O	-	R7	P165	634
GND	P142	T7	P166	-
I/O	-	R6	P167	637
I/O	-	R5	P168	640
I/O	P143	V5	P169	643
I/O	P144	V4	P170	646
I/O	P145	U5	P171	649
I/O	P146	T6	P172	652
I/O (D1)	P147	V3	P173	655
I/O ($\overline{RCLK}$, RDY/$\overline{BUSY}$)	P148	V2	P174	658
I/O	-	-	-	661
I/O	-	-	-	664
I/O	P149	U4	P175	667
I/O	P150	T5	P176	670
I/O (D0, DIN)	P151	U3	P177	673
I/O, SGCK4 (DOUT)	P152	T4	P178	676
CCLK	P153	V1	P179	-
VCC	P154	R4	P180	-
O, TDO	P159	U2	P181	0
GND	P160	R3	P182	-
I/O (A0, $\overline{WS}$)	P161	T3	P183	2
I/O, PGCK4 (A1)	P162	U1	P184	5
I/O	P163	P3	P185	8
I/O	P164	R2	P186	11
I/O (CS1, A2)	P165	T2	P187	14
I/O (A3)	P166	N3	P188	17
I/O	-	-	-	20
I/O	-	-	-	23
I/O	-	P4	P189	26
I/O	-	N4	P190	29
I/O	P167	P2	P191	32
I/O	P168	T1	P192	35
I/O	P169	R1	P193	38
I/O	P170	N2	P194	41
GND	P171	M3	P196	-
I/O	P172	P1	P197	44
I/O	P173	N1	P198	47
I/O	-	M4	P199	50
I/O	-	L4	P200	53
VCC	-	-	P201	-
I/O	-	-	-	56
I/O	-	-	-	59
I/O (A4)	P174	M2	P202	62
I/O (A5)	P175	M1	P203	65
I/O	P176	L3	P205	68
I/O	P177	L2	P206	71
I/O	P178	L1	P207	74
I/O	P179	K1	P208	77
I/O (A6)	P180	K2	P209	80
I/O (A7)	P181	K3	P210	83
GND	P182	K4	P211	-

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Additional No Connect (N.C.) Connections on HQ208 & HQ240 Packages

HQ208	HQ240
P1	P22 ‡
P3	P37 ‡
P51	P83 ‡
P52	P98 ‡
P53	P143 ‡
P54	P158 ‡
P102	P195
P104	P204 ‡
P105	P219 ‡
P107	
P155	
P156	
P157	
P158	
P206	
P207	
P208	

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‡ Pins marked with this symbol are reserved for Ground connections on future revisions of the device. These pins do not physically connect to anything on the current device revision. However, they should be externally connected to Ground, if possible.

Pin Locations for XC4025E, XC4028EX, & XC4028XL Devices

XC4025E, /28EX/XL Pad Name	HQ 208	PG 223	HQ 240	PG 299	HQ 304	BG 352	Bndry Scan
VCC	P183	J4	P212	K1	P38	VCC*	-
I/O (A8)	P184	J3	P213	K2	P37	D14	98
I/O (A9)	P185	J2	P214	K3	P36	C14	101
I/O (A19)	P186	J1	P215	K5	P35	A15	104
I/O (A18)	P187	H1	P216	K4	P34	B15	107
I/O	P188	H2	P217	J1	P33	C15	110
I/O	P189	H3	P218	J2	P32	D15	113
I/O (A10)	P190	G1	P220	H1	P31	A16	116
I/O (A11)	P191	G2	P221	J3	P30	B16	119
GND	-	-	-	-	-	GND*	-
I/O	-	-	-	J4	P29	C16	122
I/O	-	-	-	J5	P28	B17	125
I/O	-	-	-	H2	P27	C17	128
I/O	-	-	-	G1	P26	B18	131
VCC	-	-	P222	E1	P25	VCC*	-
I/O	-	H4	P223	H3	P23	C18	134
I/O	-	G4	P224	G2	P22	D17	137
I/O	P192	F1	P225	H4	P21	A20	140
I/O	P193	E1	P226	F2	P20	B19	143
GND	P194	G3	P227	F1	P19	GND*	-
I/O	-	-	-	H5	P18	C19	146
I/O	-	-	-	G3	P17	D18	149
I/O	P195	F2	P228	D1	P16	A21	152
I/O	P196	D1	P229	G4	P15	B20	155
I/O	P197	C1	P230	E2	P14	C20	158
I/O	P198	E2	P231	F3	P13	B21	161
I/O (A12)	P199	F3	P232	G5	P12	B22	164
I/O (A13)	P200	D2	P233	C1	P10	C21	167
GND	-	-	-	-	-	GND*	-
VCC	-	-	-	-	-	VCC*	-
I/O	-	-	-	F4	P9	D20	170
I/O	-	-	-	E3	P8	A23	173
I/O	-	F4	P234	D2	P7	D21	176
I/O	-	E4	P235	C2	P6	C22	179
I/O	P201	B1	P236	F5	P5	B24	182
I/O	P202	E3	P237	E4	P4	C23	185
I/O (A14)	P203	C2	P238	D3	P3	D22	188
I/O, SGCK1, GCK8 (A15)	P204	B2	P239	C3	P2	C24	191
VCC	P205	D3	P240	A2	P1	VCC*	-
GND	P2	D4	P1	B1	P304	GND*	-
I/O, PGCK1, GCK1 (A16)	P4	C3	P2	D4	P303	D23	194
I/O (A17)	P5	C4	P3	B2	P302	C25	197
I/O	P6	B3	P4	B3	P301	D24	200
I/O	P7	C5	P5	E6	P300	E23	203
I/O. TDI	P8	A2	P6	D5	P299	C26	206
I/O, TCK	P9	B4	P7	C4	P298	E24	209
I/O	-	-	-	A3	P297	F24	212
I/O	-	-	-	D6	P296	E25	215
VCC	-	-	-	-	-	VCC*	-
GND	-	-	-	-	-	GND*	-
I/O	P10	C6	P8	E7	P295	D26	218
I/O	P11	A3	P9	B4	P294	G24	221
I/O	P12	B5	P10	C5	P293	F25	224
I/O	P13	B6	P11	A4	P292	F26	227
I/O	-	D5	P12	D7	P291	H23	230
I/O	-	D6	P13	C6	P290	H24	233
I/O	-	-	-	E8	P289	G25	236
I/O	-	-	-	B5	P288	G26	239
GND	P14	C7	P14	A5	P287	GND*	-
I/O, FCLK1	P15	A4	P15	B6	P286	J23	242
I/O	P16	A5	P16	D8	P285	J24	245
I/O, TMS	P17	B7	P17	C7	P284	H25	248
I/O	P18	A6	P18	B7	P283	K23	251
VCC	-	-	P19	A6	P282	VCC*	-
I/O	-	D7	P20	C8	P280	K24	254
I/O	-	D8	P21	E9	P279	J25	257
I/O	-	-	-	A7	P278	L24	260
I/O	-	-	-	D9	P277	K25	263
GND‡	-	-	P22	-	-	GND*	-
I/O	-	-	-	B8	P276	L25	266
I/O	-	-	-	A8	P275	L26	269
I/O	P19	C8	P23	C9	P274	M23	272
I/O	P20	A7	P24	B9	P273	M24	275
I/O	P21	B8	P25	E10	P272	M25	278
I/O	P22	A8	P26	A9	P271	M26	281
I/O	P23	B9	P27	D10	P270	N24	284
I/O	P24	C9	P28	C10	P269	N25	287
GND	P25	D9	P29	A10	P268	GND*	-
VCC	P26	D10	P30	A11	P267	VCC*	-
I/O	P27	C10	P31	B10	P266	N26	290
I/O	P28	B10	P32	B11	P265	P25	293
I/O	P29	A9	P33	C11	P264	P23	296
I/O	P30	A10	P34	E11	P263	P24	299
I/O	P31	A11	P35	D11	P262	R26	302
I/O	P32	C11	P36	A12	P261	R25	305
I/O	-	-	-	B12	P260	R24	308
I/O	-	-	-	A13	P259	R23	311
GND‡	-	-	P37	-	-	GND*	-
I/O	-	-	-	C12	P258	T26	314
I/O	-	-	-	D12	P257	T25	317
I/O	-	D11	P38	E12	P256	T23	320
I/O	-	D12	P39	B13	P255	V26	323
VCC	-	-	P40	A16	P253	VCC*	-
I/O	P33	B11	P41	A14	P252	U24	326
I/O	P34	A12	P42	C13	P251	V25	329
I/O	P35	B12	P43	B14	P250	V24	332
I/O, FCLK2	P36	A13	P44	D13	P249	U23	335
GND	P37	C12	P45	A15	P248	GND*	-

XC4025E, /28EX/XL Pad Name	HQ 208	PG 223	HQ 240	PG 299	HQ 304	BG 352	Bndry Scan
I/O	-	-	-	B15	P247	Y26	338
I/O	-	-	-	E13	P246	W25	341
I/O	-	D13	P46	C14	P245	W24	344
I/O	-	D14	P47	A17	P244	V23	347
I/O	P38	B13	P48	D14	P243	AA26	350
I/O	P39	A14	P49	B16	P242	Y25	353
I/O	P40	A15	P50	C15	P241	Y24	356
I/O	P41	C13	P51	E14	P240	AA25	359
GND	-	-	-	-	-	GND*	-
VCC	-	-	-	-	-	VCC*	-
I/O	-	-	-	A18	P239	AB25	362
I/O	-	-	-	D15	P238	AA24	365
I/O	P42	B14	P52	C16	P237	Y23	368
I/O	P43	A16	P53	B17	P236	AC26	371
I/O	P44	B15	P54	B18	P235	AA23	374
I/O	P45	C14	P55	E15	P234	AB24	377
I/O	P46	A17	P56	D16	P233	AD25	380
I/O, SGCK2, GCK2	P47	B16	P57	C17	P232	AC24	383
O (M1)	P48	C15	P58	A20	P231	AB23	386
GND	P49	D15	P59	A19	P230	GND*	-
I (M0)	P50	A18	P60	C18	P229	AD24	389
VCC	P55	D16	P61	B20	P228	VCC*	-
I (M2)	P56	C16	P62	D17	P227	AC23	390
I/O, PGCK2, GCK3	P57	B17	P63	B19	P226	AE24	391
I/O (HDC)	P58	E16	P64	C19	P225	AD23	394
I/O	P59	C17	P65	F16	P224	AC22	397
I/O	P60	D17	P66	E17	P223	AF24	400
I/O	P61	B18	P67	D18	P222	AD22	403
I/O ($\overline{\text{LDC}}$)	P62	E17	P68	C20	P221	AE23	406
I/O	-	-	-	F17	P220	AE22	409
I/O	-	-	-	G16	P219	AF23	412
VCC	-	-	-	-	-	VCC*	-
GND	-	-	-	-	-	GND*	-
I/O	P63	F16	P69	D19	P218	AD20	415
I/O	P64	C18	P70	E18	P217	AE21	418
I/O	P65	D18	P71	D20	P216	AF21	421
I/O	P66	F17	P72	G17	P215	AC19	424
I/O	-	E15	P73	F18	P214	AD19	427
I/O	-	F15	P74	H16	P213	AE20	430
I/O	-	-	-	E19	P212	AF20	433
I/O	-	-	-	F19	P211	AC18	436
GND	P67	G16	P75	E20	P210	GND*	-
I/O	P68	E18	P76	H17	P209	AD18	439
I/O	P69	F18	P77	G18	P208	AE19	442
I/O	P70	G17	P78	G19	P207	AC17	445
I/O	P71	G18	P79	H18	P206	AD17	448
VCC	-	-	P80	F20	P204	VCC*	-
I/O	P72	H16	P81	J16	P203	AE18	451
I/O	P73	H17	P82	G20	P202	AF18	454

XC4025E, /28EX/XL Pad Name	HQ 208	PG 223	HQ 240	PG 299	HQ 304	BG 352	Bndry Scan
I/O	-	-	-	J17	P201	AE17	457
I/O	-	-	-	H19	P200	AE16	460
GND‡	-	-	P83	-	-	GND*	-
I/O	-	-	-	H20	P199	AF16	463
I/O	-	-	-	J18	P198	AC15	466
I/O	-	G15	P84	J19	P197	AD15	469
I/O	-	H15	P85	K16	P196	AE15	472
I/O	P74	H18	P86	J20	P195	AF15	475
I/O	P75	J18	P87	K17	P194	AD14	478
I/O	P76	J17	P88	K18	P193	AE14	481
I/O ($\overline{\text{INIT}}$)	P77	J16	P89	K19	P192	AF14	484
VCC	P78	J15	P90	L20	P191	VCC*	-
GND	P79	K15	P91	K20	P190	GND*	-
I/O	P80	K16	P92	L19	P189	AE13	487
I/O	P81	K17	P93	L18	P188	AC13	490
I/O	P82	K18	P94	L16	P187	AD13	493
I/O	P83	L18	P95	L17	P186	AF12	496
I/O	P84	L17	P96	M20	P185	AE12	499
I/O	P85	L16	P97	M19	P184	AD12	502
I/O	-	-	-	N20	P183	AC12	505
I/O	-	-	-	M18	P182	AF11	508
GND‡	-	-	P98	-	-	GND*	-
I/O	-	-	-	M17	P181	AE11	511
I/O	-	-	-	M16	P180	AD11	514
I/O	-	L15	P99	N19	P179	AF9	517
I/O	-	M15	P100	P20	P178	AD10	520
VCC	-	-	P101	T20	P177	VCC*	-
I/O	P86	M18	P102	N18	P175	AE9	523
I/O	P87	M17	P103	P19	P174	AD9	526
I/O	P88	N18	P104	N17	P173	AC10	529
I/O	P89	P18	P105	R19	P172	AF7	532
GND	P90	M16	P106	R20	P171	GND*	-
I/O	-	-	-	N16	P170	AE8	535
I/O	-	-	-	P18	P169	AD8	538
I/O	-	N15	P107	U20	P168	AC9	541
I/O	-	P15	P108	P17	P167	AF6	544
I/O	P91	N17	P109	T19	P166	AE7	547
I/O	P92	R18	P110	R18	P165	AD7	550
I/O	P93	T18	P111	P16	P164	AE6	553
I/O	P94	P17	P112	V20	P163	AE5	556
GND	-	-	-	-	-	GND*	-
VCC	-	-	-	-	-	VCC*	-
I/O	-	-	-	R17	P162	AD6	559
I/O	-	-	-	T18	P161	AC7	562
I/O	P95	N16	P113	U19	P160	AF4	565
I/O	P96	T17	P114	V19	P159	AF3	568
I/O	P97	R17	P115	R16	P158	AD5	571
I/O	P98	P16	P116	T17	P157	AE3	574
I/O	P99	U18	P117	U18	P156	AD4	577
I/O, SGCK3, GCK4	P100	T16	P118	X20	P155	AC5	580

XC4025E, /28EX/XL Pad Name	HQ 208	PG 223	HQ 240	PG 299	HQ 304	BG 352	Bndry Scan
GND	P101	R16	P119	W20	P154	GND*	-
DONE	P103	U17	P120	V18	P153	AD3	-
VCC	P106	R15	P121	X19	P152	VCC*	-
$\overline{\text{PROGRAM}}$	P108	V18	P122	U17	P151	AC4	-
I/O (D7)	P109	T15	P123	W19	P150	AD2	583
I/O, PGCK3, GCK5	P110	U16	P124	W18	P149	AC3	586
I/O	P111	T14	P125	T15	P148	AB4	589
I/O	P112	U15	P126	U16	P147	AD1	592
I/O	-	R14	P127	V17	P146	AA4	595
I/O	-	R13	P128	X18	P145	AA3	598
I/O	-	-	-	U15	P144	AB2	601
I/O	-	-	-	T14	P143	AC1	604
VCC	-	-	-	-	-	VCC*	-
GND	-	-	-	-	-	GND*	-
I/O (D6)	P113	V17	P129	W17	P142	Y3	607
I/O	P114	V16	P130	V16	P141	AA2	610
I/O	P115	T13	P131	X17	P140	AA1	613
I/O	P116	U14	P132	U14	P139	W4	616
I/O	P117	V15	P133	V15	P138	W3	619
I/O	P118	V14	P134	T13	P137	Y2	622
I/O	-	-	-	W16	P136	Y1	625
I/O	-	-	-	W15	P135	V4	628
GND	P119	T12	P135	X16	P134	GND*	-
I/O	-	R12	P136	U13	P133	V3	631
I/O	-	R11	P137	V14	P132	W2	634
I/O, FCLK3	P120	U13	P138	W14	P131	U4	637
I/O	P121	V13	P139	V13	P130	U3	640
VCC	-	-	P140	X15	P129	VCC*	-
I/O (D5)	P122	U12	P141	T12	P127	V2	643
I/O ($\overline{\text{CS0}}$)	P123	V12	P142	X14	P126	V1	646
GND‡	-	-	P143	-	-	-	-
I/O	-	-	-	U12	P125	U2	649
I/O	-	-	-	W13	P124	T2	652
GND	-	-	-	-	-	GND*	-
I/O	-	-	-	X13	P123	T1	655
I/O	-	-	-	V12	P122	R4	658
I/O	P124	T11	P144	W12	P121	R3	661
I/O	P125	U11	P145	T11	P120	R2	664
I/O	P126	V11	P146	X12	P119	R1	667
I/O	P127	V10	P147	U11	P118	P3	670
I/O (D4)	P128	U10	P148	V11	P117	P2	673
I/O	P129	T10	P149	W11	P116	P1	676
VCC	P130	R10	P150	X10	P115	VCC*	-
GND	P131	R9	P151	X11	P114	GND*	-
I/O (D3)	P132	T9	P152	W10	P113	N2	679
I/O ($\overline{\text{RS}}$)	P133	U9	P153	V10	P112	N4	682
I/O	P134	V9	P154	T10	P111	N3	685
I/O	P135	V8	P155	U10	P110	M1	688
I/O	P136	U8	P156	X9	P109	M2	691
I/O	P137	T8	P157	W9	P108	M3	694

XC4025E, /28EX/XL Pad Name	HQ 208	PG 223	HQ 240	PG 299	HQ 304	BG 352	Bndry Scan
I/O	-	-	-	X8	P107	M4	697
I/O	-	-	-	V9	P106	L1	700
GND‡	-	-	P158	-	-	GND*	-
I/O	-	-	-	U9	P105	L2	703
I/O	-	-	-	T9	P104	L3	706
I/O (D2)	P138	V7	P159	W8	P103	J1	709
I/O	P139	U7	P160	X7	P102	K3	712
VCC	-	-	P161	X5	P101	VCC*	-
I/O	P140	V6	P162	V8	P99	J2	715
I/O, FCLK4	P141	U6	P163	W7	P98	J3	718
I/O	-	R8	P164	U8	P97	K4	721
I/O	-	R7	P165	W6	P96	G1	724
GND	P142	T7	P166	X6	P95	GND*	-
I/O	-	-	-	T8	P94	H2	727
I/O	-	-	-	V7	P93	H3	730
I/O	-	R6	P167	X4	P92	J4	733
I/O	-	R5	P168	U7	P91	F1	736
I/O	P143	V5	P169	W5	P90	G2	739
I/O	P144	V4	P170	V6	P89	G3	742
I/O	P145	U5	P171	T7	P88	F2	745
I/O	P146	T6	P172	X3	P87	E2	748
GND	-	-	-	-	-	GND*	-
VCC	-	-	-	-	-	VCC*	-
I/O (D1)	P147	V3	P173	U6	P86	F3	751
I/O ($\overline{\text{RCLK}}$, $\overline{\text{RDY}}$/$\overline{\text{BUSY}}$)	P148	V2	P174	V5	P85	G4	754
I/O	-	-	-	W4	P84	D2	757
I/O	-	-	-	W3	P83	F4	760
I/O	P149	U4	P175	T6	P82	E3	763
I/O	P150	T5	P176	U5	P81	C2	766
I/O (D0, DIN)	P151	U3	P177	V4	P80	D3	769
I/O, SGCK4, GCK6 (DOUT)	P152	T4	P178	X1	P79	E4	772
CCLK	P153	V1	P179	V3	P78	C3	-
VCC	P154	R4	P180	W1	P77	VCC*	-
O, TDO	P159	U2	P181	U4	P76	D4	0
GND	P160	R3	P182	X2	P75	GND*	-
I/O (A0, $\overline{\text{WS}}$)	P161	T3	P183	W2	P74	B3	2
I/O, PGCK4, GCK7 (A1)	P162	U1	P184	V2	P73	C4	5
I/O	P163	P3	P185	R5	P72	D5	8
I/O	P164	R2	P186	T4	P71	A3	11
I/O (CS1, A2)	P165	T2	P187	U3	P70	D6	14
I/O (A3)	P166	N3	P188	V1	P69	C6	17
I/O	-	-	-	R4	P68	B5	20
I/O	-	-	-	P5	P67	A4	23
VCC	-	-	-	-	-	VCC*	-
GND	-	-	-	-	-	GND*	-
I/O	-	P4	P189	U2	P66	C7	26

XC4025E, /28EX/XL Pad Name	HQ 208	PG 223	HQ 240	PG 299	HQ 304	BG 352	Bndry Scan
I/O	-	N4	P190	T3	P65	B6	29
I/O	P167	P2	P191	U1	P64	A6	32
I/O	P168	T1	P192	P4	P63	D8	35
I/O	P169	R1	P193	R3	P62	B7	38
I/O	P170	N2	P194	N5	P61	A7	41
I/O	-	-	P195	T2	P60	D9	44
I/O	-	-	-	R2	P59	C9	47
GND	P171	M3	P196	T1	P58	GND*	-
I/O	P172	P1	P197	N4	P57	B8	50
I/O	P173	N1	P198	P3	P56	D10	53
I/O	-	M4	P199	P2	P55	C10	56
I/O	-	L4	P200	N3	P54	B9	59
VCC	-	-	P201	R1	P52	VCC*	-
I/O	-	-	-	M5	P51	A9	62
I/O	-	-	-	P1	P50	D11	65
I/O	-	-	-	M4	P49	B11	68
I/O	-	-	-	N2	P48	A11	71
GND	-	-	-	-	-	GND*	-
I/O (A4)	P174	M2	P202	N1	P47	D12	74
I/O (A5)	P175	M1	P203	M3	P46	C12	77
I/O	P176	L3	P205	M2	P45	B12	80
I/O	P177	L2	P206	L5	P44	A12	83
I/O (A21)	P178	L1	P207	M1	P43	C13	86
I/O (A20)	P179	K1	P208	L4	P42	B13	89
I/O (A6)	P180	K2	P209	L3	P41	A13	92
I/O (A7)	P181	K3	P210	L2	P40	B14	95
GND	P182	K4	P211	L1	P39	GND*	-

4/2/96

Pads labelled GND* are internally bonded to a Ground plane within the BG352 package. They have no direct connection to any package pin.

Pads labelled VCC* are internally bonded to a Vcc plane within the BG352 package. They have no direct connection to any package pin.

Pads labelled GND‡ should be connected to Ground if possible; however, they can be left unconnected if necessary for compatibility with other devices.

Additional No Connect (N.C.) Connections on HQ208 Package

N.C.	N.C.
P1	P107
P3	P155
P51	P156
P52	P157
P53	P158
P54	P206
P102	P207
P104	P208
P105	

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Additional Ground (GND) Connections on HQ240 Package

GND
P204
P219

3/21/96

The Ground (GND) package pins in the above table should be externally connected to Ground if possible; however, they can be left unconnected if necessary for compatibility with other devices.

Additional No Connect (N.C.) Connections on HQ304 Package

N.C.
P11
P24
P53
P100
P128
P176
P205
P254
P281

3/21/96

Note: In XC4025 (no extension) devices in the HQ304 package, P101 is a No Connect (N.C.) pin. P101 is Vcc in XC4025E/L and XC4028EX/XL devices. Where necessary for compatibility, this pin can be left unconnected.

Additional No Connect, Vcc & Ground Connections on BG352 Package

N.C.	VCC	GND
A18	A10	A1
A24	A17	A2
B4	B2	A5
B10	B25	A8
B23	D7	A14
C1	D13	A19
C5	D19	A22
C8	G23	A25
C11	H4	A26
D1	K1	B1
D16	K26	B26
D25	N23	E1
F23	P4	E26
J26	U1	H1
K2	U26	H26
L4	W23	N1
L23	Y4	P26
T3	AC8	W1
T4	AC14	W26
T24	AC20	AB1
U25	AE2	AB26
AB3	AE25	AE1
AC2	AF10	AE26
AC6	AF17	AF1
AC11		AF2
AC16		AF5
AC21		AF8
AC25		AF13
AD16		AF19
AD21		AF22
AD26		AF25
AE4		AF26
AE10		

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Pin Locations for XC4036EX/XL Devices

XC4036EX/XL Pad Name	HQ304	PG411	BG432	Bndry Scan
GND	P304	GND*	GND*	-
I/O, GCK1 (A16)	P303	H8	D29	218
I/O (A17)	P302	F6	C30	221
I/O	P301	B4	E28	224
I/O	P300	D4	E29	227
I/O, TDI	P299	B2	D30	230
I/O, TCK	P298	G9	D31	233
I/O	-	F8	E30	236
I/O	-	C5	E31	239
I/O	P297	A7	G28	242
I/O	P296	A5	G29	245
VCC	-	VCC*	VCC*	-
GND	-	GND*	GND*	-
I/O	P295	B8	H28	248
I/O	P294	C9	H29	251
I/O	P293	E9	G30	254
I/O	P292	F12	H30	257
I/O	P291	D10	J28	260
I/O	P290	B10	J29	263
I/O	P289	F10	H31	266
I/O	P288	F14	J30	269
GND	P287	GND*	GND*	-
I/O, FCLK1	P286	C11	K28	272
I/O	P285	B12	K29	275
I/O, TMS	P284	E11	K30	278
I/O	P283	E15	K31	281
VCC	P282	VCC*	VCC*	-
I/O	P280	F16	L29	284
I/O	P279	C13	L30	287
I/O	-	B14	M29	290
I/O	-	E17	M31	293
I/O	P278	E13	N31	296
I/O	P277	A15	N28	299
GND	-	GND*	GND*	-
VCC	-	VCC*	VCC*	-
I/O	P276	B16	P30	302
I/O	P275	D16	P28	305
I/O	P274	D18	P29	308
I/O	P273	A17	R31	311
I/O	P272	E19	R30	314
I/O	P271	B18	R28	317
I/O	P270	C17	R29	320
I/O	P269	C19	T31	323
GND	P268	GND*	GND*	-
VCC	P267	VCC*	VCC*	-
I/O	P266	F20	T30	326
I/O	P265	B20	T29	329
I/O	P264	C21	U31	332
I/O	P263	B22	U30	335
I/O	P262	E21	U28	338
I/O	P261	D22	U29	341
I/O	P260	A23	V30	344
I/O	P259	B24	V29	347
VCC	-	VCC*	VCC*	-
GND	-	GND*	GND*	-
I/O	P258	A25	W30	350
I/O	P257	D24	W29	353
I/O	-	B26	Y30	356
I/O	-	A27	Y29	359
I/O	P256	C27	Y28	362
I/O	P255	F24	AA30	365
VCC	P253	VCC*	VCC*	-
I/O	P252	E25	AA29	368
I/O	P251	E27	AB31	371
I/O	P250	B28	AB30	374
I/O, FCLK2	P249	C29	AB29	377
GND	P248	GND*	GND*	-
I/O	P247	F26	AB28	380
I/O	P246	D28	AC30	383
I/O	P245	B30	AC29	386
I/O	P244	E29	AC28	389
I/O	P243	F28	AD29	392
I/O	P242	F30	AD28	395
I/O	P241	C31	AE30	398
I/O	P240	E31	AE29	401
GND	-	GND*	GND*	-
VCC	-	VCC*	VCC*	-
I/O	P239	B32	AF31	404
I/O	P238	A33	AE28	407
I/O	P237	A35	AG31	410
I/O	P236	F32	AF28	413
I/O	-	C35	AG30	416
I/O	-	B38	AG29	419
I/O	P235	E33	AH31	422
I/O	P234	G31	AG28	425
I/O	P233	H32	AH30	428
I/O, GCK2	P232	B36	AJ30	431
O (M1)	P231	A39	AH29	434
GND	P230	GND*	GND*	-
I (M0)	P229	E35	AH28	437
VCC	P228	VCC*	VCC*	-
I (M2)	P227	G33	AJ28	438

XC4036EX/XL Pad Name	HQ304	PG411	BG432	Bndry Scan
I/O, GCK3	P226	D36	AK29	439
I/O (HDC)	P225	C37	AH27	442
I/O	P224	F34	AK28	445
I/O	P223	J33	AJ27	448
I/O	P222	D38	AL28	451
I/O ($\overline{LDC}$)	P221	G35	AH26	454
I/O	-	E39	AL27	457
I/O	-	K34	AH25	460
I/O	P220	F38	AK26	463
I/O	P219	G37	AL26	466
VCC	-	VCC*	VCC*	-
GND	-	GND*	GND*	-
I/O	P218	H38	AH24	469
I/O	P217	J37	AJ25	472
I/O	P216	G39	AK25	475
I/O	P215	M34	AJ24	478
I/O	P214	N35	AL24	481
I/O	P213	P34	AH22	484
I/O	P212	J35	AJ23	487
I/O	P211	L37	AK23	490
GND	P210	GND*	GND*	-
I/O	P209	M38	AJ22	493
I/O	P208	R35	AK22	496
I/O	P207	H36	AL22	499
I/O	P206	T34	AJ21	502
VCC	P204	VCC*	VCC*	-
I/O	P203	N37	AH20	505
I/O	P202	N39	AK21	508
I/O	-	U35	AK20	511
I/O	-	R39	AJ19	514
I/O	P201	M36	AL20	517
I/O	P200	V34	AH18	520
GND	-	GND*	GND*	-
VCC	-	VCC*	VCC*	-
I/O	P199	R37	AK19	523
I/O	P198	T38	AJ18	526
I/O	P197	T36	AL19	529
I/O	P196	V36	AK18	532
I/O	P195	U37	AH17	535
I/O	P194	U39	AJ17	538
I/O	P193	V38	AJ16	541
I/O ($\overline{INIT}$)	P192	W37	AK16	544
VCC	P191	VCC*	VCC*	-
GND	P190	GND*	GND*	-
I/O	P189	Y34	AL16	547
I/O	P188	AC37	AH15	550
I/O	P187	AB38	AK15	553

XC4036EX/XL Pad Name	HQ304	PG411	BG432	Bndry Scan
I/O	P186	AD36	AJ14	556
I/O	P185	AA35	AH14	559
I/O	P184	AE37	AK14	562
I/O	P183	AB36	AL13	565
I/O	P182	AD38	AK13	568
VCC	-	VCC*	VCC*	-
GND	-	GND*	GND*	-
I/O	P181	AB34	AJ13	571
I/O	P180	AE39	AH13	574
I/O	-	AM36	AL12	577
I/O	-	AC35	AK12	580
I/O	P179	AG39	AH12	583
I/O	P178	AG37	AJ11	586
VCC	P177	VCC*	VCC*	-
I/O	P175	AD34	AL10	589
I/O	P174	AN39	AK10	592
I/O	P173	AE35	AJ10	595
I/O	P172	AH38	AK9	598
GND	P171	GND*	GND*	-
I/O	P170	AJ37	AL8	601
I/O	P169	AG35	AH10	604
I/O	P168	AF34	AJ9	607
I/O	P167	AH36	AK8	610
I/O	P166	AK36	AK7	613
I/O	P165	AM34	AL6	616
I/O	P164	AH34	AJ7	619
I/O	P163	AJ35	AH8	622
GND	-	GND*	GND*	-
VCC	-	VCC*	VCC*	-
I/O	P162	AL37	AK6	625
I/O	P161	AT38	AL5	628
I/O	P160	AM38	AH7	631
I/O	P159	AN37	AJ6	634
I/O	-	AK34	AK5	637
I/O	-	AR39	AL4	640
I/O	P158	AN35	AK4	643
I/O	P157	AL33	AH5	646
I/O	P156	AV38	AK3	649
I/O, GCK4	P155	AT36	AJ4	652
GND	P154	GND*	GND*	-
DONE	P153	AR35	AH4	-
VCC	P152	VCC*	VCC*	-
$\overline{PROGRAM}$	P151	AN33	AH3	-
I/O (D7)	P150	AM32	AJ2	655
I/O, GCK5	P149	AP34	AG4	658
I/O	P148	AW39	AG3	661
I/O	P147	AN31	AH2	664

XC4036EX/XL Pad Name	HQ304	PG411	BG432	Bndry Scan
I/O	-	AV36	AH1	667
I/O	-	AR33	AF4	670
I/O	P146	AP32	AF3	673
I/O	P145	AU35	AG2	676
I/O	P144	AW33	AE3	679
I/O	P143	AU33	AF2	682
VCC	-	VCC*	VCC*	-
GND	-	GND*	GND*	-
I/O (D6)	P142	AV32	AF1	685
I/O	P141	AU31	AD4	688
I/O	P140	AR31	AD3	691
I/O	P139	AP28	AE2	694
I/O	P138	AT32	AC3	697
I/O	P137	AV30	AD1	700
I/O	P136	AR29	AC2	703
I/O	P135	AP26	AB4	706
GND	P134	GND*	GND*	-
I/O	P133	AU29	AB3	709
I/O	P132	AV28	AB2	712
I/O, FCLK3	P131	AT28	AB1	715
I/O	P130	AR25	AA3	718
VCC	P129	VCC*	VCC*	-
I/O (D5)	P127	AP24	AA2	721
I/O ($\overline{CS0}$)	P126	AU27	Y2	724
I/O	-	AR27	Y4	727
I/O	-	AW27	Y3	730
I/O	P125	AT24	W4	733
I/O	P124	AR23	W3	736
GND	-	GND*	GND*	-
VCC	-	VCC*	VCC*	-
I/O	P123	AP22	V4	739
I/O	P122	AV24	V3	742
I/O	P121	AU23	U1	745
I/O	P120	AT22	U2	748
I/O	P119	AR21	U4	751
I/O	P118	AV22	U3	754
I/O (D4)	P117	AP20	T1	757
I/O	P116	AU21	T2	760
VCC	P115	VCC*	VCC*	-
GND	P114	GND*	GND*	-
I/O (D3)	P113	AU19	T3	763
I/O ($\overline{RS}$)	P112	AV20	R1	766
I/O	P111	AV18	R2	769
I/O	P110	AR19	R4	772
I/O	P109	AT18	R3	775
I/O	P108	AW17	P2	778
I/O	P107	AV16	P3	781

XC4036EX/XL Pad Name	HQ304	PG411	BG432	Bndry Scan
I/O	P106	AP18	P4	784
VCC	-	VCC*	VCC*	-
GND	-	GND*	GND*	-
I/O	P105	AR17	N3	787
I/O	P104	AT16	N4	790
I/O	-	AV14	M1	793
I/O	-	AW13	M2	796
I/O (D2)	P103	AR15	L2	799
I/O	P102	AP16	L3	802
VCC	P101	VCC*	VCC*	-
I/O	P99	AV12	K1	805
I/O, FCLK4	P98	AR13	K2	808
I/O	P97	AU11	K3	811
I/O	P96	AT12	K4	814
GND	P95	GND*	GND*	-
I/O	P94	AP14	J2	817
I/O	P93	AR11	J3	820
I/O	P92	AV10	J4	823
I/O	P91	AT8	H1	826
I/O	P90	AT10	H2	829
I/O	P89	AP10	H3	832
I/O	P88	AP12	H4	835
I/O	P87	AR9	G2	838
GND	-	GND*	GND*	-
VCC	-	VCC*	VCC*	-
I/O (D1)	P86	AU7	G4	841
I/O ($\overline{RCLK}$, RDY/$\overline{BUSY}$)	P85	AW7	F2	844
I/O	-	AW5	F3	847
I/O	-	AV6	E1	850
I/O	P84	AR7	E3	853
I/O	P83	AV4	D1	856
I/O	P82	AN9	E4	859
I/O	P81	AW1	D2	862
I/O (D0, DIN)	P80	AP6	C2	865
I/O, GCK6 (DOUT)	P79	AU3	D3	868
CCLK	P78	AR5	D4	-
VCC	P77	VCC*	VCC*	-
O, TDO	P76	AN7	C4	0
GND	P75	GND*	GND*	-
I/O (A0, $\overline{WS}$)	P74	AT4	B3	2
I/O, GCK7 (A1)	P73	AV2	D5	5
I/O	P72	AM8	B4	8
I/O	P71	AL7	C5	11
I/O	-	AR3	B5	14
I/O	-	AR1	C6	17
I/O (CS1, A2)	P70	AK6	A5	20

XC4036EX/XL Pad Name	HQ304	PG411	BG432	Bndry Scan
I/O (A3)	P69	AN3	D7	23
I/O	P68	AM6	B6	26
I/O	P67	AM2	A6	29
VCC	-	VCC*	VCC*	-
GND	-	GND*	GND*	-
I/O	P66	AL3	D8	32
I/O	P65	AH6	C7	35
I/O	P64	AP2	B7	38
I/O	P63	AK4	D9	41
I/O	P62	AG5	D10	44
I/O	P61	AF6	C9	47
I/O	P60	AL5	B9	50
I/O	P59	AJ3	C10	53
GND	P58	GND*	GND*	-
I/O	P57	AH2	B10	56
I/O	P56	AE5	A10	59
I/O	P55	AM4	C11	62
I/O	P54	AD6	D12	65
VCC	P52	VCC*	VCC*	-
I/O	P51	AG3	B11	68
I/O	P50	AG1	C12	71
I/O	-	AC5	C13	74
I/O	-	AE1	A12	77
I/O	P49	AH4	D14	80
I/O	P48	AB6	B13	83
GND	-	GND*	GND*	-
VCC	-	VCC*	VCC*	-
I/O (A4)	P47	AD2	C14	86
I/O (A5)	P46	AB4	A13	89
I/O	P45	AE3	B14	92
I/O	P44	AC1	D15	95
I/O (A21)	P43	AD4	C15	98
I/O (A20)	P42	AA5	B15	101
I/O (A6)	P41	AA3	B16	104
I/O (A7)	P40	Y6	A16	107
GND	P39	GND*	GND*	-
VCC	P38	VCC*	VCC*	-
I/O (A8)	P37	W3	D17	110
I/O (A9)	P36	Y2	A17	113
I/O (A19)	P35	V4	C18	116
I/O (A18)	P34	T2	D18	119
I/O	P33	U1	B18	122
I/O	P32	V6	A19	125
I/O (A10)	P31	U3	B19	128
I/O (A11)	P30	R1	C19	131
VCC	-	VCC*	VCC*	-
GND	-	GND*	GND*	-

XC4036EX/XL Pad Name	HQ304	PG411	BG432	Bndry Scan
I/O	P29	U5	D19	134
I/O	P28	T4	A20	137
I/O	-	P2	B20	140
I/O	-	N1	C20	143
I/O	P27	R5	C21	146
I/O	P26	M2	A22	149
VCC	P25	VCC*	VCC*	-
I/O	P23	L3	B22	152
I/O	P22	T6	C22	155
I/O	P21	N5	B23	158
I/O	P20	M4	A24	161
GND	P19	GND*	GND*	-
I/O	P18	K2	D22	164
I/O	P17	K4	C23	167
I/O	P16	P6	B24	170
I/O	P15	M6	C24	173
I/O	P14	J3	A26	176
I/O	P13	H2	C25	179
I/O (A12)	P12	H4	D24	182
I/O (A13)	P10	G3	B26	185
GND	-	GND*	GND*	-
VCC	-	VCC*	VCC*	-
I/O	P9	K6	A27	188
I/O	P8	G1	D25	191
I/O	-	E1	C26	194
I/O	-	E3	B27	197
I/O	P7	J7	C27	200
I/O	P6	H6	B28	203
I/O	P5	C3	D27	206
I/O	P4	D2	B29	209
I/O (A14)	P3	E5	C28	212
I/O, GCK8 (A15)	P2	G7	D28	215
VCC	P1	VCC*	VCC*	-

4/2/96

Pads labelled GND* are internally bonded to a Ground plane within the associated package. They have no direct connection to any package pin.

Pads labelled VCC* are internally bonded to a Vcc plane within the associated package. They have no direct connection to any package pin.

Additional No Connect (N.C.) Connections on HQ304 Package

N.C.	N.C.
P11	P176
P24	P205
P53	P254
P100	P281
P128	

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Additional No Connect, Vcc & Ground Connections on PG411 Package

N.C.	N.C.	VCC	GND
A13	AA37	A3	A9
B6	AB2	A11	A19
B34	AC3	A21	A29
C7	AC39	A31	A37
C15	AF2	C39	C1
C23	AF38	D6	D14
C25	AJ5	F36	D20
C33	AK2	J1	D26
D8	AK38	L39	D34
D12	AL35	W1	F4
D30	AN1	AA39	J39
D32	AN5	AJ1	L1
E7	AP8	AL39	P4
E23	AP30	AP4	P36
E37	AP38	AT34	W39
F2	AR37	AU1	Y4
F18	AT2	AW9	Y36
F22	AT30	AW19	AA1
G5	AU5	AW29	AF4
H34	AU9	AW37	AF36
J5	AU13		AJ39
K36	AU15		AL1
K38	AU17		AP36
L5	AU25		AT6
L35	AU37		AT14
N3	AV8		AT20
P38	AV26		AT26
R3	AV34		AU39
V2	AW15		AW3
W5	AW23		AW11
W35	AW25		AW21
Y38	AW35		AW31

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Additional No Connect, Vcc & Ground Connections on BG432 Package

N.C.	N.C.	VCC	GND
A4	AG1	A1	A2
A8	AH6	A11	A3
A15	AH9	A21	A7
A28	AH19	A31	A9
B8	AH23	C3	A14
B12	AJ5	C29	A18
B17	AJ8	D11	A23
B21	AJ12	D21	A25
B25	AJ15	L1	A29
C8	AJ20	L4	A30
C16	AJ26	L28	B1
C17	AK11	L31	B2
D6	AK17	AA1	B30
D13	AK24	AA4	B31
D20	AK27	AA28	C1
D23	AL15	AA31	C31
D26	AL17	AH11	D16
E2		AH21	G1
F1		AJ3	G31
F4		AJ29	J1
F28		AL1	J31
F29		AL11	P1
F30		AL21	P31
F31		AL31	T4
G3			T28
M3			V1
M4			V31
M28			AC1
M30			AC31
N1			AE1
N2			AE31
N29			AH16
N30			AJ1
V2			AJ31
V28			AK1
W1			AK2
W2			AK30
W28			AK31
W31			AL2
Y1			AL3
Y31			AL7
AC4			AL9
AD2			AL14
AD30			AL18
AD31			AL23
AE4			AL25
AF29			AL29
AF30			AL30

3/22/96

Pin Locations for XC4044EX/XL Devices

XC4044EX/XL Pad Name	PG411	BG432	Bndry Scan
GND	GND*	GND*	-
I/O, GCK1 (A16)	H8	D29	242
I/O (A17)	F6	C30	245
I/O	B4	E28	248
I/O	D4	E29	251
I/O, TDI	B2	D30	254
I/O, TCK	G9	D31	257
I/O	F8	E30	260
I/O	C5	E31	263
I/O	A7	G28	266
I/O	A5	G29	269
VCC	VCC*	VCC*	-
GND	GND*	GND*	-
I/O	C7	F30	272
I/O	D8	F31	275
I/O	B8	H28	278
I/O	C9	H29	281
I/O	E9	G30	284
I/O	F12	H30	287
I/O	D10	J28	290
I/O	B10	J29	293
I/O	F10	H31	296
I/O	F14	J30	299
GND	GND*	GND*	-
I/O, FCLK1	C11	K28	302
I/O	B12	K29	305
I/O, TMS	E11	K30	308
I/O	E15	K31	311
VCC	VCC*	VCC*	-
I/O	F16	L29	314
I/O	C13	L30	317
I/O	B14	M29	320
I/O	E17	M31	323
I/O	E13	N31	326
I/O	A15	N28	329
GND	GND*	GND*	-
VCC	VCC*	VCC*	-
I/O	F18	N29	332
I/O	C15	N30	335
I/O	B16	P30	338
I/O	D16	P28	341
I/O	D18	P29	344
I/O	A17	R31	347
I/O	E19	R30	350
I/O	B18	R28	353
I/O	C17	R29	356
I/O	C19	T31	359
GND	GND*	GND*	-
VCC	VCC*	VCC*	-
I/O	F20	T30	362
I/O	B20	T29	365
I/O	C21	U31	368
I/O	B22	U30	371
I/O	E21	U28	374
I/O	D22	U29	377
I/O	A23	V30	380
I/O	B24	V29	383
I/O	C23	V28	386
I/O	F22	W31	389
VCC	VCC*	VCC*	-
GND	GND*	GND*	-
I/O	A25	W30	392
I/O	D24	W29	395
I/O	B26	Y30	398
I/O	A27	Y29	401
I/O	C27	Y28	404
I/O	F24	AA30	407
VCC	VCC*	VCC*	-
I/O	E25	AA29	410
I/O	E27	AB31	413
I/O	B28	AB30	416
I/O, FCLK2	C29	AB29	419
GND	GND*	GND*	-
I/O	F26	AB28	422
I/O	D28	AC30	425
I/O	B30	AC29	428
I/O	E29	AC28	431
I/O	D30	AD31	434
I/O	D32	AD30	437
I/O	F28	AD29	440
I/O	F30	AD28	443
I/O	C31	AE30	446
I/O	E31	AE29	449
GND	GND*	GND*	-
VCC	VCC*	VCC*	-
I/O	B32	AF31	452
I/O	A33	AE28	455
I/O	A35	AG31	458
I/O	F32	AF28	461
I/O	C35	AG30	464
I/O	B38	AG29	467
I/O	E33	AH31	470
I/O	G31	AG28	473
I/O	H32	AH30	476
I/O, GCK2	B36	AJ30	479
O (M1)	A39	AH29	482
GND	GND*	GND*	-
I (M0)	E35	AH28	485
VCC	VCC*	VCC*	-
I (M2)	G33	AJ28	486
I/O, GCK3	D36	AK29	487
I/O (HDC)	C37	AH27	490

XC4044EX/XL Pad Name	PG411	BG432	Bndry Scan
I/O	F34	AK28	493
I/O	J33	AJ27	496
I/O	D38	AL28	499
I/O ($\overline{LDC}$)	G35	AH26	502
I/O	E39	AL27	505
I/O	K34	AH25	508
I/O	F38	AK26	511
I/O	G37	AL26	514
VCC	VCC*	VCC*	-
GND	GND*	GND*	-
I/O	H38	AH24	517
I/O	J37	AJ25	520
I/O	G39	AK25	523
I/O	M34	AJ24	526
I/O	K36	AH23	529
I/O	K38	AK24	532
I/O	N35	AL24	535
I/O	P34	AH22	538
I/O	J35	AJ23	541
I/O	L37	AK23	544
GND	GND*	GND*	-
I/O	M38	AJ22	547
I/O	R35	AK22	550
I/O	H36	AL22	553
I/O	T34	AJ21	556
VCC	VCC*	VCC*	-
I/O	N37	AH20	559
I/O	N39	AK21	562
I/O	U35	AK20	565
I/O	R39	AJ19	568
I/O	M36	AL20	571
I/O	V34	AH18	574
GND	GND*	GND*	-
VCC	VCC*	VCC*	-
I/O	R37	AK19	577
I/O	T38	AJ18	580
I/O	T36	AL19	583
I/O	V36	AK18	586
I/O	U37	AH17	589
I/O	U39	AJ17	592
I/O	W35	AK17	595
I/O	AC39	AL17	598
I/O	V38	AJ16	601
I/O ($\overline{INIT}$)	W37	AK16	604
VCC	VCC*	VCC*	-
GND	GND*	GND*	-
I/O	Y34	AL16	607
I/O	AC37	AH15	610
I/O	Y38	AL15	613
I/O	AA37	AJ15	616
I/O	AB38	AK15	619
I/O	AD36	AJ14	622

XC4044EX/XL Pad Name	PG411	BG432	Bndry Scan
I/O	AA35	AH14	625
I/O	AE37	AK14	628
I/O	AB36	AL13	631
I/O	AD38	AK13	634
VCC	VCC*	VCC*	-
GND	GND*	GND*	-
I/O	AB34	AJ13	637
I/O	AE39	AH13	640
I/O	AM36	AL12	643
I/O	AC35	AK12	646
I/O	AG39	AH12	649
I/O	AG37	AJ11	652
VCC	VCC*	VCC*	-
I/O	AD34	AL10	655
I/O	AN39	AK10	658
I/O	AE35	AJ10	661
I/O	AH38	AK9	664
GND	GND*	GND*	-
I/O	AJ37	AL8	667
I/O	AG35	AH10	670
I/O	AF34	AJ9	673
I/O	AH36	AK8	676
I/O	AK38	AJ8	679
I/O	AP38	AH9	682
I/O	AK36	AK7	685
I/O	AM34	AL6	688
I/O	AH34	AJ7	691
I/O	AJ35	AH8	694
GND	GND*	GND*	-
VCC	VCC*	VCC*	-
I/O	AL37	AK6	697
I/O	AT38	AL5	700
I/O	AM38	AH7	703
I/O	AN37	AJ6	706
I/O	AK34	AK5	709
I/O	AR39	AL4	712
I/O	AN35	AK4	715
I/O	AL33	AH5	718
I/O	AV38	AK3	721
I/O, GCK4	AT36	AJ4	724
GND	GND*	GND*	-
DONE	AR35	AH4	-
VCC	VCC*	VCC*	-
$\overline{PROGRAM}$	AN33	AH3	-
I/O (D7)	AM32	AJ2	727
I/O, GCK5	AP34	AG4	730
I/O	AW39	AG3	733
I/O	AN31	AH2	736
I/O	AV36	AH1	739
I/O	AR33	AF4	742
I/O	AP32	AF3	745
I/O	AU35	AG2	748

XC4044EX/XL Pad Name	PG411	BG432	Bndry Scan
I/O	AW33	AE3	751
I/O	AU33	AF2	754
VCC	VCC*	VCC*	-
GND	GND*	GND*	-
I/O (D6)	AV32	AF1	757
I/O	AU31	AD4	760
I/O	AR31	AD3	763
I/O	AP28	AE2	766
I/O	AP30	AD2	769
I/O	AT30	AC4	772
I/O	AT32	AC3	775
I/O	AV30	AD1	778
I/O	AR29	AC2	781
I/O	AP26	AB4	784
GND	GND*	GND*	-
I/O	AU29	AB3	787
I/O	AV28	AB2	790
I/O, FCLK3	AT28	AB1	793
I/O	AR25	AA3	796
VCC	VCC*	VCC*	-
I/O (D5)	AP24	AA2	799
I/O ($\overline{CS0}$)	AU27	Y2	802
I/O	AR27	Y4	805
I/O	AW27	Y3	808
I/O	AT24	W4	811
I/O	AR23	W3	814
GND	GND*	GND*	-
VCC	VCC*	VCC*	-
I/O	AW25	W2	817
I/O	AW23	V2	820
I/O	AP22	V4	823
I/O	AV24	V3	826
I/O	AU23	U1	829
I/O	AT22	U2	832
I/O	AR21	U4	835
I/O	AV22	U3	838
I/O (D4)	AP20	T1	841
I/O	AU21	T2	844
VCC	VCC*	VCC*	-
GND	GND*	GND*	-
I/O (D3)	AU19	T3	847
I/O ($\overline{RS}$)	AV20	R1	850
I/O	AV18	R2	853
I/O	AR19	R4	856
I/O	AT18	R3	859
I/O	AW17	P2	862
I/O	AV16	P3	865
I/O	AP18	P4	868
I/O	AU17	N1	871
I/O	AW15	N2	874
VCC	VCC*	VCC*	-
GND	GND*	GND*	-

XC4044EX/XL Pad Name	PG411	BG432	Bndry Scan
I/O	AR17	N3	877
I/O	AT16	N4	880
I/O	AV14	M1	883
I/O	AW13	M2	886
I/O (D2)	AR15	L2	889
I/O	AP16	L3	892
VCC	VCC*	VCC*	-
I/O	AV12	K1	895
I/O, FCLK4	AR13	K2	898
I/O	AU11	K3	901
I/O	AT12	K4	904
GND	GND*	GND*	-
I/O	AP14	J2	907
I/O	AR11	J3	910
I/O	AV10	J4	913
I/O	AT8	H1	916
I/O	AT10	H2	919
I/O	AP10	H3	922
I/O	AP12	H4	925
I/O	AR9	G2	928
I/O	AU9	G3	931
I/O	AV8	F1	934
GND	GND*	GND*	-
VCC	VCC*	VCC*	-
I/O (D1)	AU7	G4	937
I/O ($\overline{RCLK}$, RDY/$\overline{BUSY}$)	AW7	F2	940
I/O	AW5	F3	943
I/O	AV6	E1	946
I/O	AR7	E3	949
I/O	AV4	D1	952
I/O	AN9	E4	955
I/O	AW1	D2	958
I/O (D0, DIN)	AP6	C2	961
I/O, GCK6 (DOUT)	AU3	D3	964
CCLK	AR5	D4	-
VCC	VCC*	VCC*	-
O, TDO	AN7	C4	0
GND	GND*	GND*	-
I/O (A0, $\overline{WS}$)	AT4	B3	2
I/O, GCK7 (A1)	AV2	D5	5
I/O	AM8	B4	8
I/O	AL7	C5	11
I/O	AR3	B5	14
I/O	AR1	C6	17
I/O (CS1, A2)	AK6	A5	20
I/O (A3)	AN3	D7	23
I/O	AM6	B6	26
I/O	AM2	A6	29
VCC	VCC*	VCC*	-
GND	GND*	GND*	-

XC4044EX/XL Pad Name	PG411	BG432	Bndry Scan
I/O	AL3	D8	32
I/O	AH6	C7	35
I/O	AP2	B7	38
I/O	AK4	D9	41
I/O	AN1	B8	44
I/O	AK2	A8	47
I/O	AG5	D10	50
I/O	AF6	C9	53
I/O	AL5	B9	56
I/O	AJ3	C10	59
GND	GND*	GND*	-
I/O	AH2	B10	62
I/O	AE5	A10	65
I/O	AM4	C11	68
I/O	AD6	D12	71
VCC	VCC*	VCC*	-
I/O	AG3	B11	74
I/O	AG1	C12	77
I/O	AC5	C13	80
I/O	AE1	A12	83
I/O	AH4	D14	86
I/O	AB6	B13	89
GND	GND*	GND*	-
VCC	VCC*	VCC*	-
I/O (A4)	AD2	C14	92
I/O (A5)	AB4	A13	95
I/O	AE3	B14	98
I/O	AC1	D15	101
I/O (A21)	AD4	C15	104
I/O (A20)	AA5	B15	107
I/O	AB2	A15	110
I/O	AC3	C16	113
I/O (A6)	AA3	B16	116
I/O (A7)	Y6	A16	119
GND	GND*	GND*	-
VCC	VCC*	VCC*	-
I/O (A8)	W3	D17	122
I/O (A9)	Y2	A17	125
I/O	V2	C17	128
I/O	W5	B17	131
I/O (A19)	V4	C18	134
I/O (A18)	T2	D18	137
I/O	U1	B18	140
I/O	V6	A19	143
I/O (A10)	U3	B19	146
I/O (A11)	R1	C19	149
VCC	VCC*	VCC*	-
GND	GND*	GND*	-
I/O	U5	D19	152
I/O	T4	A20	155
I/O	P2	B20	158
I/O	N1	C20	161

XC4044EX/XL Pad Name	PG411	BG432	Bndry Scan
I/O	R5	C21	164
I/O	M2	A22	167
VCC	VCC*	VCC*	-
I/O	L3	B22	170
I/O	T6	C22	173
I/O	N5	B23	176
I/O	M4	A24	179
GND	GND*	GND*	-
I/O	K2	D22	182
I/O	K4	C23	185
I/O	P6	B24	188
I/O	M6	C24	191
I/O	L5	D23	194
I/O	J5	B25	197
I/O	J3	A26	200
I/O	H2	C25	203
I/O (A12)	H4	D24	206
I/O (A13)	G3	B26	209
GND	GND*	GND*	-
VCC	VCC*	VCC*	-
I/O	K6	A27	212
I/O	G1	D25	215
I/O	E1	C26	218
I/O	E3	B27	221
I/O	J7	C27	224
I/O	H6	B28	227
I/O	C3	D27	230
I/O	D2	B29	233
I/O (A14)	E5	C28	236
I/O, GCK8 (A15)	G7	D28	239
VCC	VCC*	VCC*	-

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Pads labelled GND* are internally bonded to a Ground plane within the associated package. They have no direct connection to any package pin.

Pads labelled VCC* are internally bonded to a Vcc plane within the associated package. They have no direct connection to any package pin.

Additional No Connect, Vcc & Ground Connections on PG411 Package

N.C.	VCC	GND
A13	A3	A9
B6	A11	A19
B34	A21	A29
C25	A31	A37
C33	C39	C1
D12	D6	D14
E7	F36	D20
E23	J1	D26
E37	L39	D34
F2	W1	F4
G5	AA39	J39
H34	AJ1	L1
L35	AL39	P4
N3	AP4	P36
P38	AT34	W39
R3	AU1	Y4
AF2	AW9	Y36
AF38	AW19	AA1
AJ5	AW29	AF4
AL35	AW37	AF36
AN5		AJ39
AP8		AL1
AR37		AP36
AT2		AT6
AU5		AT14
AU13		AT20
AU15		AT26
AU25		AU39
AU37		AW3
AV26		AW11
AV34		AW21
AW35		AW31

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Additional No Connect, Vcc & Ground Connections on BG432 Package

N.C.	VCC	GND
A4	A1	A2
A28	A11	A3
B12	A21	A7
B21	A31	A9
C8	C3	A14
D6	C29	A18
D13	D11	A23
D20	D21	A25
D26	L1	A29
E2	L4	A30
F4	L28	B1
F28	L31	B2
F29	AA1	B30
M3	AA4	B31
M4	AA28	C1
M28	AA31	C31
M30	AH11	D16
W1	AH21	G1
W28	AJ3	G31
Y1	AJ29	J1
Y31	AL1	J31
AE4	AL11	P1
AF29	AL21	P31
AF30	AL31	T4
AG1		T28
AH6		V1
AH19		V31
AJ5		AC1
AJ12		AC31
AJ20		AE1
AJ26		AE31
AK11		AH16
AK27		AJ1
		AJ31
		AK1
		AK2
		AK30
		AK31
		AL2
		AL3
		AL7
		AL9
		AL14
		AL18
		AL23
		AL25
		AL29
		AL30

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Pin Locations for XC4052XL Devices

XC4052XL Pad Name	BG432	Bndry Scan
GND	GND*	-
I/O, GCK1 (A16)	D29	266
I/O (A17)	C30	269
I/O	E28	272
I/O	E29	275
I/O, TDI	D30	278
I/O, TCK	D31	281
GND	GND*	-
I/O	F28	284
I/O	F29	287
I/O	E30	290
I/O	E31	293
I/O	G28	296
I/O	G29	299
VCC	VCC*	-
GND	GND*	-
I/O	F30	302
I/O	F31	305
I/O	H28	308
I/O	H29	311
I/O	G30	314
I/O	H30	317
GND	GND*	-
I/O	J28	320
I/O	J29	323
I/O	H31	326
I/O	J30	329
GND	GND*	-
I/O, FCLK1	K28	332
I/O	K29	335
I/O, TMS	K30	338
I/O	K31	341
VCC	VCC*	-
I/O	L29	344
I/O	L30	347
GND	GND*	-
I/O	M30	350
I/O	M28	353
I/O	M29	356
I/O	M31	359
I/O	N31	362
I/O	N28	365
GND	GND*	-
VCC	VCC*	-
I/O	N29	368
I/O	N30	371
I/O	P30	374
I/O	P28	377
I/O	P29	380
I/O	R31	383
GND	GND*	-

XC4052XL Pad Name	BG432	Bndry Scan
I/O	R30	386
I/O	R28	389
I/O	R29	392
I/O	T31	395
GND	GND*	-
VCC	VCC*	-
I/O	T30	398
I/O	T29	401
I/O	U31	404
I/O	U30	407
GND	GND*	-
I/O	U28	410
I/O	U29	413
I/O	V30	416
I/O	V29	419
I/O	V28	422
I/O	W31	425
VCC	VCC*	-
GND	GND*	-
I/O	W30	428
I/O	W29	431
I/O	W28	434
I/O	Y31	437
I/O	Y30	440
I/O	Y29	443
GND	GND*	-
I/O	Y28	446
I/O	AA30	449
VCC	VCC*	-
I/O	AA29	452
I/O	AB31	455
I/O	AB30	458
I/O, FCLK2	AB29	461
GND	GND*	-
I/O	AB28	464
I/O	AC30	467
I/O	AC29	470
I/O	AC28	473
GND	GND*	-
I/O	AD31	476
I/O	AD30	479
I/O	AD29	482
I/O	AD28	485
I/O	AE30	488
I/O	AE29	491
GND	GND*	-
VCC	VCC*	-
I/O	AF31	494
I/O	AE28	497
I/O	AF30	500
I/O	AF29	503
I/O	AG31	506

XC4052XL Pad Name	BG432	Bndry Scan
I/O	AF28	509
GND	GND*	-
I/O	AG30	512
I/O	AG29	515
I/O	AH31	518
I/O	AG28	521
I/O	AH30	524
I/O, GCK2	AJ30	527
O (M1)	AH29	530
GND	GND*	-
I (M0)	AH28	533
VCC	VCC*	-
I (M2)	AJ28	534
I/O, GCK3	AK29	535
I/O (HDC)	AH27	538
I/O	AK28	541
I/O	AJ27	544
I/O	AL28	547
I/O ($\overline{LDC}$)	AH26	550
GND	GND*	-
I/O	AK27	553
I/O	AJ26	556
I/O	AL27	559
I/O	AH25	562
I/O	AK26	565
I/O	AL26	568
VCC	VCC*	-
GND	GND*	-
I/O	AH24	571
I/O	AJ25	574
I/O	AK25	577
I/O	AJ24	580
I/O	AH23	583
I/O	AK24	586
GND	GND*	-
I/O	AL24	589
I/O	AH22	592
I/O	AJ23	595
I/O	AK23	598
GND	GND*	-
I/O	AJ22	601
I/O	AK22	604
I/O	AL22	607
I/O	AJ21	610
VCC	VCC*	-
I/O	AH20	613
I/O	AK21	616
GND	GND*	-
I/O	AJ20	619
I/O	AH19	622
I/O	AK20	625
I/O	AJ19	628

XC4052XL Pad Name	BG432	Bndry Scan
I/O	AL20	631
I/O	AH18	634
GND	GND*	-
VCC	VCC*	-
I/O	AK19	637
I/O	AJ18	640
I/O	AL19	643
I/O	AK18	646
I/O	AH17	649
I/O	AJ17	652
GND	GND*	-
I/O	AK17	655
I/O	AL17	658
I/O	AJ16	661
I/O ($\overline{INIT}$)	AK16	664
VCC	VCC*	-
GND	GND*	-
I/O	AL16	667
I/O	AH15	670
I/O	AL15	673
I/O	AJ15	676
GND	GND*	-
I/O	AK15	679
I/O	AJ14	682
I/O	AH14	685
I/O	AK14	688
I/O	AL13	691
I/O	AK13	694
VCC	VCC*	-
GND	GND*	697
I/O	AJ13	700
I/O	AH13	703
I/O	AL12	706
I/O	AK12	709
I/O	AJ12	712
I/O	AK11	715
GND	GND*	-
I/O	AH12	718
I/O	AJ11	721
VCC	VCC*	-
I/O	AL10	724
I/O	AK10	727
I/O	AJ10	730
I/O	AK9	733
GND	GND*	-
I/O	AL8	736
I/O	AH10	739
I/O	AJ9	742
I/O	AK8	745
GND	GND*	-
I/O	AJ8	748
I/O	AH9	751

XC4052XL Pad Name	BG432	Bndry Scan
I/O	AK7	754
I/O	AL6	757
I/O	AJ7	760
I/O	AH8	763
GND	GND*	-
VCC	VCC*	-
I/O	AK6	766
I/O	AL5	769
I/O	AH7	772
I/O	AJ6	775
I/O	AK5	778
I/O	AL4	781
GND	GND*	-
I/O	AH6	784
I/O	AJ5	787
I/O	AK4	790
I/O	AH5	793
I/O	AK3	796
I/O, GCK4	AJ4	799
GND	GND*	-
DONE	AH4	-
VCC	VCC*	-
$\overline{\text{PROGRAM}}$	AH3	-
I/O (D7)	AJ2	802
I/O, GCK5	AG4	805
I/O	AG3	808
I/O	AH2	811
I/O	AH1	814
I/O	AF4	817
GND	GND*	-
I/O	AF3	820
I/O	AG2	823
I/O	AG1	826
I/O	AE4	829
I/O	AE3	832
I/O	AF2	835
VCC	VCC*	-
GND	GND*	-
I/O (D6)	AF1	838
I/O	AD4	841
I/O	AD3	844
I/O	AE2	847
I/O	AD2	850
I/O	AC4	853
GND	GND*	-
I/O	AC3	856
I/O	AD1	859
I/O	AC2	862
I/O	AB4	865
GND	GND*	-
I/O	AB3	868
I/O	AB2	871

XC4052XL Pad Name	BG432	Bndry Scan
I/O, FCLK3	AB1	874
I/O	AA3	877
VCC	VCC*	-
I/O (D5)	AA2	880
I/O ($\overline{\text{CS0}}$)	Y2	883
GND	GND*	-
I/O	Y4	886
I/O	Y3	889
I/O	Y1	892
I/O	W1	895
I/O	W4	898
I/O	W3	901
GND	GND*	-
VCC	VCC*	-
I/O	W2	904
I/O	V2	907
I/O	V4	910
I/O	V3	913
I/O	U1	916
I/O	U2	919
GND	GND*	-
I/O	U4	922
I/O	U3	925
I/O (D4)	T1	928
I/O	T2	931
VCC	VCC*	-
GND	GND*	-
I/O (D3)	T3	934
I/O ($\overline{\text{RS}}$)	R1	937
I/O	R2	940
I/O	R4	943
GND	GND*	-
I/O	R3	946
I/O	P2	949
I/O	P3	952
I/O	P4	955
I/O	N1	958
I/O	N2	961
VCC	VCC*	-
GND	GND*	-
I/O	N3	964
I/O	N4	967
I/O	M1	970
I/O	M2	973
I/O	M3	976
I/O	M4	979
GND	GND*	-
I/O (D2)	L2	982
I/O	L3	985
VCC	VCC*	-
I/O	K1	988
I/O, FCLK4	K2	991

XC4052XL Pad Name	BG432	Bndry Scan
I/O	K3	994
I/O	K4	997
GND	GND*	-
I/O	J2	1000
I/O	J3	1003
I/O	J4	1006
I/O	H1	1009
GND	GND*	-
I/O	H2	1012
I/O	H3	1015
I/O	H4	1018
I/O	G2	1021
I/O	G3	1024
I/O	F1	1027
GND	GND*	-
VCC	VCC*	-
I/O (D1)	G4	1030
I/O ($\overline{RCLK}$, RDY/$\overline{BUSY}$)	F2	1033
I/O	F3	1036
I/O	E1	1039
I/O	F4	1042
I/O	E2	1045
GND	GND*	-
I/O	E3	1048
I/O	D1	1051
I/O	E4	1054
I/O	D2	1057
I/O (D0. DIN)	C2	1060
I/O, GCK6 (DOUT)	D3	1063
CCLK	D4	-
VCC	VCC*	-
O, TDO	C4	0
GND	GND*	-
I/O (A0, $\overline{WS}$)	B3	2
I/O, GCK7 (A1)	D5	5
I/O	B4	8
I/O	C5	11
I/O	A4	14
I/O	D6	17
GND	GND*	-
I/O	B5	20
I/O	C6	23
I/O (CS1, A2)	A5	26
I/O (A3)	D7	29
I/O	B6	32
I/O	A6	35
VCC	VCC*	-
GND	GND*	-
I/O	D8	38
I/O	C7	41
I/O	B7	44
I/O	D9	47

XC4052XL Pad Name	BG432	Bndry Scan
I/O	B8	50
I/O	A8	53
GND	GND*	-
I/O	D10	56
I/O	C9	59
I/O	B9	62
I/O	C10	65
GND	GND*	-
I/O	B10	68
I/O	A10	71
I/O	C11	74
I/O	D12	77
VCC	VCC*	-
I/O	B11	80
I/O	C12	83
GND	GND*	-
I/O	D13	86
I/O	B12	89
I/O	C13	92
I/O	A12	95
I/O	D14	98
I/O	B13	101
GND	GND*	-
VCC	VCC*	-
I/O (A4)	C14	104
I/O (A5)	A13	107
I/O	B14	110
I/O	D15	113
I/O (A21)	C15	116
I/O (A20)	B15	119
GND	GND*	-
I/O	A15	122
I/O	C16	125
I/O (A6)	B16	128
I/O (A7)	A16	131
GND	GND*	-
VCC	VCC*	-
I/O (A8)	D17	134
I/O (A9)	A17	137
I/O	C17	140
I/O	B17	143
GND	GND*	-
I/O (A19)	C18	146
I/O (A18)	D18	149
I/O	B18	152
I/O	A19	155
I/O (A10)	B19	158
I/O (A11)	C19	161
VCC	VCC*	-
GND	GND*	-
I/O	D19	164
I/O	A20	167

XC4052XL Pad Name	BG432	Bndry Scan
I/O	B20	170
I/O	C20	173
I/O	B21	176
I/O	D20	179
GND	GND*	-
I/O	C21	182
I/O	A22	185
VCC	VCC*	-
I/O	B22	188
I/O	C22	191
I/O	B23	194
I/O	A24	197
GND	GND*	-
I/O	D22	200
I/O	C23	203
I/O	B24	206
I/O	C24	209
GND	GND*	-
I/O	D23	212
I/O	B25	215
I/O	A26	218
I/O	C25	221
I/O (A12)	D24	224
I/O (A13)	B26	227
GND	GND*	-
VCC	VCC*	-
I/O	A27	230
I/O	D25	233
I/O	C26	236
I/O	B27	239
I/O	A28	242
I/O	D26	245
GND	GND*	-
I/O	C27	248
I/O	B28	251
I/O	D27	254
I/O	B29	257
I/O (A14)	C28	260
I/O, GCK8 (A15)	D28	263
VCC	VCC*	-

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Pads labelled GND* are internally bonded to a Ground plane within the associated package. They have no direct connection to any package pin.

Pads labelled VCC* are internally bonded to a Vcc plane within the associated package. They have no direct connection to any package pin.

Additional No Connect, Vcc & Ground Connections on BG432 Package

N.C.	VCC	GND
C8	A1	A2
	A11	A3
	A21	A7
	A31	A9
	C3	A14
	C29	A18
	D11	A23
	D21	A25
	L1	A29
	L4	A30
	L28	B1
	L31	B2
	AA1	B30
	AA4	B31
	AA28	C1
	AA31	C31
	AH11	D16
	AH21	G1
	AJ3	G31
	AJ29	J1
	AL1	J31
	AL11	P1
	AL21	P31
	AL31	T4
		T28
		V1
		V31
		AC1
		AC31
		AE1
		AE31
		AH16
		AJ1
		AJ31
		AK1
		AK2
		AK30
		AK31
		AL2
		AL3
		AL7
		AL9
		AL14
		AL18
		AL23
		AL25
		AL29
		AL30

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Package-Specific Pinout Tables

PC84 Package Pinouts

Pin	XC4003E	XC4005E XC4005L	XC4006E	XC4008E	XC4010E XC4010L
P1	GND	GND	GND	GND	GND
P2	VCC	VCC	VCC	VCC	VCC
P3	I/O (A8)	I/O (A8)	I/O (A8)	I/O (A8)	I/O (A8)
P4	I/O (A9)	I/O (A9)	I/O (A9)	I/O (A9)	I/O (A9)
P5	I/O (A10)	I/O (A10)	I/O (A10)	I/O (A10)	I/O (A10)
P6	I/O (A11)	I/O (A11)	I/O (A11)	I/O (A11)	I/O (A11)
P7	I/O (A12)	I/O (A12)	I/O (A12)	I/O (A12)	I/O (A12)
P8	I/O (A13)	I/O (A13)	I/O (A13)	I/O (A13)	I/O (A13)
P9	I/O (A14)	I/O (A14)	I/O (A14)	I/O (A14)	I/O (A14)
P10	I/O, SGCK1 (A15)	I/O, SGCK1 (A15)	I/O, SGCK1 (A15)	I/O, SGCK1 (A15)	I/O, SGCK1 (A15)
P11	VCC	VCC	VCC	VCC	VCC
P12	GND	GND	GND	GND	GND
P13	I/O, PGCK1 (A16)	I/O, PGCK1 (A16)	I/O, PGCK1 (A16)	I/O, PGCK1 (A16)	I/O, PGCK1 (A16)
P14	I/O (A17)	I/O (A17)	I/O (A17)	I/O (A17)	I/O (A17)
P15	I/O, TDI	I/O, TDI	I/O, TDI	I/O, TDI	I/O, TDI
P16	I/O, TCK	I/O, TCK	I/O, TCK	I/O, TCK	I/O, TCK
P17	I/O, TMS	I/O, TMS	I/O, TMS	I/O, TMS	I/O, TMS
P18	I/O	I/O	I/O	I/O	I/O
P19	I/O	I/O	I/O	I/O	I/O
P20	I/O	I/O	I/O	I/O	I/O
P21	GND	GND	GND	GND	GND
P22	VCC	VCC	VCC	VCC	VCC
P23	I/O	I/O	I/O	I/O	I/O
P24	I/O	I/O	I/O	I/O	I/O
P25	I/O	I/O	I/O	I/O	I/O
P26	I/O	I/O	I/O	I/O	I/O
P27	I/O	I/O	I/O	I/O	I/O
P28	I/O	I/O	I/O	I/O	I/O
P29	I/O, SCGK2	I/O, SCGK2	I/O, SCGK2	I/O, SCGK2	I/O, SCGK2
P30	O (M1)	O (M1)	O (M1)	O (M1)	O (M1)
P31	GND	GND	GND	GND	GND
P32	I (M0)	I (M0)	I (M0)	I (M0)	I (M0)
P33	VCC	VCC	VCC	VCC	VCC
P34	I (M2)	I (M2)	I (M2)	I (M2)	I (M2)
P35	I/O, PGCK2	I/O, PGCK2	I/O, PGCK2	I/O, PGCK2	I/O, PGCK2
P36	I/O (HDC)	I/O (HDC)	I/O (HDC)	I/O (HDC)	I/O (HDC)
P37	I/O ($\overline{LDC}$)	I/O ($\overline{LDC}$)	I/O ($\overline{LDC}$)	I/O ($\overline{LDC}$)	I/O ($\overline{LDC}$)
P38	I/O	I/O	I/O	I/O	I/O
P39	I/O	I/O	I/O	I/O	I/O
P40	I/O	I/O	I/O	I/O	I/O
P41	I/O ($\overline{INIT}$)	I/O ($\overline{INIT}$)	I/O ($\overline{INIT}$)	I/O ($\overline{INIT}$)	I/O ($\overline{INIT}$)
P42	VCC	VCC	VCC	VCC	VCC
P43	GND	GND	GND	GND	GND
P44	I/O	I/O	I/O	I/O	I/O
P45	I/O	I/O	I/O	I/O	I/O
P46	I/O	I/O	I/O	I/O	I/O
P47	I/O	I/O	I/O	I/O	I/O
P48	I/O	I/O	I/O	I/O	I/O
P49	I/O	I/O	I/O	I/O	I/O
P50	I/O	I/O	I/O	I/O	I/O
P51	I/O, SGCK3	I/O, SGCK3	I/O, SGCK3	I/O, SGCK3	I/O, SGCK3
P52	GND	GND	GND	GND	GND
P53	DONE	DONE	DONE	DONE	DONE
P54	VCC	VCC	VCC	VCC	VCC
P55	$\overline{PRO-GRAM}$	$\overline{PRO-GRAM}$	$\overline{PRO-GRAM}$	$\overline{PRO-GRAM}$	$\overline{PRO-GRAM}$
P56	I/O (D7)	I/O (D7)	I/O (D7)	I/O (D7)	I/O (D7)
P57	I/O, PGCK3	I/O, PGCK3	I/O, PGCK3	I/O, PGCK3	I/O, PGCK3
P58	I/O (D6)	I/O (D6)	I/O (D6)	I/O (D6)	I/O (D6)
P59	I/O (D5)	I/O (D5)	I/O (D5)	I/O (D5)	I/O (D5)
P60	I/O ($\overline{CS0}$)	I/O ($\overline{CS0}$)	I/O ($\overline{CS0}$)	I/O ($\overline{CS0}$)	I/O ($\overline{CS0}$)
P61	I/O (D4)	I/O (D4)	I/O (D4)	I/O (D4)	I/O (D4)
P62	I/O	I/O	I/O	I/O	I/O
P63	VCC	VCC	VCC	VCC	VCC
P64	GND	GND	GND	GND	GND
P65	I/O (D3)	I/O (D3)	I/O (D3)	I/O (D3)	I/O (D3)
P66	I/O ($\overline{RS}$)	I/O ($\overline{RS}$)	I/O ($\overline{RS}$)	I/O ($\overline{RS}$)	I/O ($\overline{RS}$)
P67	I/O (D2)	I/O (D2)	I/O (D2)	I/O (D2)	I/O (D2)
P68	I/O	I/O	I/O	I/O	I/O
P69	I/O (D1)	I/O (D1)	I/O (D1)	I/O (D1)	I/O (D1)
P70	I/O ($\overline{RCLK}$, RDY/ $\overline{BUSY}$)	I/O ($\overline{RCLK}$, RDY/ $\overline{BUSY}$)	I/O ($\overline{RCLK}$, RDY/ $\overline{BUSY}$)	I/O ($\overline{RCLK}$, RDY/ $\overline{BUSY}$)	I/O ($\overline{RCLK}$, RDY/ $\overline{BUSY}$)
P71	I/O (D0, DIN)	I/O (D0, DIN)	I/O (D0, DIN)	I/O (D0, DIN)	I/O (D0, DIN)
P72	I/O, SGCK4 (DOUT)	I/O, SGCK4 (DOUT)	I/O, SGCK4 (DOUT)	I/O, SGCK4 (DOUT)	I/O, SGCK4 (DOUT)
P73	CCLK	CCLK	CCLK	CCLK	CCLK
P74	VCC	VCC	VCC	VCC	VCC
P75	O, TDO	O, TDO	O, TDO	O, TDO	O, TDO
P76	GND	GND	GND	GND	GND
P77	I/O (A0, $\overline{WS}$)	I/O (A0, $\overline{WS}$)	I/O (A0, $\overline{WS}$)	I/O (A0, $\overline{WS}$)	I/O (A0, $\overline{WS}$)
P78	I/O, PGCK4 (A1)	I/O, PGCK4 (A1)	I/O, PGCK4 (A1)	I/O, PGCK4 (A1)	I/O, PGCK4 (A1)
P79	I/O (CS1, A2)	I/O (CS1, A2)	I/O (CS1, A2)	I/O (CS1, A2)	I/O (CS1, A2)
P80	I/O (A3)	I/O (A3)	I/O (A3)	I/O (A3)	I/O (A3)
P81	I/O (A4)	I/O (A4)	I/O (A4)	I/O (A4)	I/O (A4)
P82	I/O (A5)	I/O (A5)	I/O (A5)	I/O (A5)	I/O (A5)
P83	I/O (A6)	I/O (A6)	I/O (A6)	I/O (A6)	I/O (A6)
P84	I/O (A7)	I/O (A7)	I/O (A7)	I/O (A7)	I/O (A7)

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PQ100 Package Pinouts

PQ100 Pin	XC4003E	XC4005E
P1	I/O (A14)	I/O (A14)
P2	I/O, SGCK1 (A15)	I/O, SGCK1 (A15)
P3	VCC	VCC
P4	GND	GND
P5	I/O, PGCK1 (A16)	I/O, PGCK1 (A16)
P6	I/O (A17)	I/O (A17)
P7	I/O, TDI	I/O, TDI
P8	I/O, TCK	I/O, TCK
P9	I/O, TMS	I/O, TMS
P10	I/O	I/O
P11	I/O	I/O
P12	I/O	I/O
P13	I/O	I/O
P14	GND	GND
P15	VCC	VCC
P16	I/O	I/O
P17	I/O	I/O
P18	I/O	I/O
P19	I/O	I/O
P20	I/O	I/O
P21	I/O	I/O
P22	I/O	I/O
P23	I/O	I/O
P24	I/O, SCGK2	I/O, SCGK2
P25	O (M1)	O (M1)
P26	GND	GND
P27	I (M0)	I (M0)
P28	VCC	VCC
P29	I (M2)	I (M2)
P30	I/O, PGCK2	I/O, PGCK2
P31	I/O (HDC)	I/O (HDC)
P32	I/O	I/O
P33	I/O ($\overline{\text{LDC}}$)	I/O ($\overline{\text{LDC}}$)
P34	I/O	I/O
P35	I/O	I/O
P36	I/O	I/O
P37	I/O	I/O
P38	I/O	I/O
P39	I/O ($\overline{\text{INIT}}$)	I/O ($\overline{\text{INIT}}$)
P40	VCC	VCC
P41	GND	GND
P42	I/O	I/O
P43	I/O	I/O
P44	I/O	I/O
P45	I/O	I/O
P46	I/O	I/O
P47	I/O	I/O
P48	I/O	I/O
P49	I/O	I/O
P50	I/O	I/O
P51	I/O, SGCK3	I/O, SGCK3
P52	GND	GND
P53	DONE	DONE
P54	VCC	VCC
P55	$\overline{\text{PROGRAM}}$	$\overline{\text{PROGRAM}}$
P56	I/O (D7)	I/O (D7)
P57	I/O, PGCK3	I/O, PGCK3
P58	I/O (D6)	I/O (D6)
P59	I/O	I/O
P60	I/O (D5)	I/O (D5)
P61	I/O ($\overline{\text{CS0}}$)	I/O ($\overline{\text{CS0}}$)
P62	I/O	I/O
P63	I/O	I/O
P64	I/O (D4)	I/O (D4)
P65	I/O	I/O
P66	VCC	VCC
P67	GND	GND
P68	I/O (D3)	I/O (D3)
P69	I/O ($\overline{\text{RS}}$)	I/O ($\overline{\text{RS}}$)
P70	I/O	I/O
P71	I/O (D2)	I/O (D2)
P72	I/O	I/O
P73	I/O (D1)	I/O (D1)
P74	I/O ($\overline{\text{RCLK}}$, RDY/$\overline{\text{BUSY}}$)	I/O ($\overline{\text{RCLK}}$, RDY/$\overline{\text{BUSY}}$)
P75	I/O (D0, DIN)	I/O (D0, DIN)
P76	I/O, SGCK4 (DOUT)	I/O, SGCK4 (DOUT)
P77	CCLK	CCLK
P78	VCC	VCC
P79	O, TDO	O, TDO
P80	GND	GND
P81	I/O (A0, $\overline{\text{WS}}$)	I/O (A0, $\overline{\text{WS}}$)
P82	I/O, PGCK4 (A1)	I/O, PGCK4 (A1)
P83	I/O (CS1, A2)	I/O (CS1, A2)
P84	I/O (A3)	I/O (A3)
P85	I/O (A4)	I/O (A4)
P86	I/O (A5)	I/O (A5)
P87	I/O	I/O
P88	I/O	I/O
P89	I/O (A6)	I/O (A6)
P90	I/O (A7)	I/O (A7)
P91	GND	GND
P92	VCC	VCC
P93	I/O (A8)	I/O (A8)
P94	I/O (A9)	I/O (A9)
P95	I/O	I/O
P96	I/O	I/O
P97	I/O (A10)	I/O (A10)
P98	I/O (A11)	I/O (A11)
P99	I/O (A12)	I/O (A12)
P100	I/O (A13)	I/O (A13)

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VQ100 Package Pinouts

VQ100 Pin	XC4003E
P1	GND
P2	I/O, PGCK1 (A16)
P3	I/O (A17)
P4	I/O, TDI
P5	I/O, TCK
P6	I/O, TMS
P7	I/O
P8	I/O
P9	I/O
P10	I/O
P11	GND
P12	VCC
P13	I/O
P14	I/O
P15	I/O
P16	I/O
P17	I/O
P18	I/O
P19	I/O
P20	I/O
P21	I/O, SCGK2
P22	O (M1)
P23	GND
P24	I (M0)
P25	VCC
P26	I (M2)
P27	I/O, PGCK2
P28	I/O (HDC)
P29	I/O
P30	I/O ($\overline{LDC}$)
P31	I/O
P32	I/O
P33	I/O
P34	I/O
P35	I/O
P36	I/O ($\overline{INIT}$)
P37	VCC
P38	GND
P39	I/O
P40	I/O
P41	I/O
P42	I/O
P43	I/O
P44	I/O
P45	I/O
P46	I/O
P47	I/O
P48	I/O, SGCK3
P49	GND
P50	DONE
P51	VCC
P52	$\overline{PROGRAM}$
P53	I/O (D7)
P54	I/O, PGCK3
P55	I/O (D6)
P56	I/O
P57	I/O (D5)
P58	I/O ($\overline{CS0}$)
P59	I/O
P60	I/O
P61	I/O (D4)
P62	I/O
P63	VCC
P64	GND
P65	I/O (D3)
P66	I/O ($\overline{RS}$)
P67	I/O
P68	I/O (D2)
P69	I/O
P70	I/O (D1)
P71	I/O ($\overline{RCLK}$, RDY/$\overline{BUSY}$)
P72	I/O (D0, DIN)
P73	I/O, SGCK4 (DOUT)
P74	CCLK
P75	VCC
P76	O, TDO
P77	GND
P78	I/O (A0, $\overline{WS}$)
P79	I/O, PGCK4 (A1)
P80	I/O (CS1, A2)
P81	I/O (A3)
P82	I/O (A4)
P83	I/O (A5)
P84	I/O
P85	I/O
P86	I/O (A6)
P87	I/O (A7)
P88	GND
P89	VCC
P90	I/O (A8)
P91	I/O (A9)
P92	I/O
P93	I/O
P94	I/O (A10)
P95	I/O (A11)
P96	I/O (A12)
P97	I/O (A13)
P98	I/O (A14)
P99	I/O, SGCK1 (A15)
P100	VCC

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PG120 Package Pinouts

PG120 Pin	XC4003E
N13	I/O, PGCK3
N12	N.C.
N11	I/O
N10	I/O ($\overline{CS0}$)
N9	I/O
N8	I/O
N7	I/O (D3)
N6	I/O ($\overline{RS}$)
N5	I/O
N4	I/O
N3	I/O ($\overline{RCLK}$, RDY/$\overline{BUSY}$)
N2	I/O (D0, DIN)
N1	I/O, PGCK4 (A1)
M13	I/O
M12	$\overline{PROGRAM}$
M11	I/O (D7)
M10	I/O (D6)
M9	I/O (D5)
M8	I/O (D4)
M7	VCC
M6	I/O
M5	I/O (D1)
M4	N.C.
M3	I/O, SGCK4 (DOUT)
M2	O, TDO
M1	N.C.
L13	I/O
L12	I/O, SGCK3
L11	DONE
L10	VCC
L9	N.C.
L8	I/O
L7	GND
L6	I/O (D2)
L5	N.C.
L4	CCLK
L3	VCC
L2	I/O (A0, $\overline{WS}$)
L1	I/O (A3)
K13	I/O
K12	N.C.
K11	GND
K3	GND
K2	I/O (CS1, A2)
K1	I/O (A5)
J13	I/O
J12	I/O
J11	N.C.
J3	N.C.
J2	I/O (A4)
J1	I/O
H13	I/O
H12	I/O
H11	I/O
H3	I/O
H2	I/O (A6)
H1	I/O (A7)
G13	I/O
G12	VCC
G11	GND
G3	VCC
G2	GND
G1	I/O (A8)
F13	I/O ($\overline{INIT}$)
F12	I/O
F11	I/O
F3	I/O (A10)
F2	I/O
F1	I/O (A9)
E13	I/O
E12	I/O
E11	N.C.
E3	N.C.
E2	N.C.
E1	I/O
D13	I/O
D12	I/O
D11	VCC
D3	I/O, SGCK1 (A15)
D2	I/O (A13)
D1	I/O (A11)
C13	I/O ($\overline{LDC}$)
C12	I/O, PGCK2
C11	I (M0)
C10	GND
C9	I/O
C8	I/O
C7	VCC
C6	I/O
C5	I/O, TDI
C4	GND
C3	VCC
C2	I/O (A14)
C1	I/O (A12)

PG120 Pin	XC4003E
B13	N.C.
B12	I (M2)
B11	O (M1)
B10	N.C.
B9	I/O
B8	I/O
B7	GND
B6	I/O
B5	I/O, TMS
B4	I/O, TCK
B3	I/O (A17)
B2	I/O, PGCK1 (A16)
B1	N.C.
A13	I/O (HDC)
A12	I/O, SCGK2
A11	I/O
A10	I/O
A9	I/O
A8	I/O
A7	I/O
A6	I/O
A5	I/O
A4	I/O
A3	N.C.
A2	N.C.
A1	N.C.

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Note: Viewed from the bottom side, the package pins start at the top row and go from the left edge to the right edge. Viewed from the top side, the pins start at the top row and go from the right edge to the left edge.

TQ144 Package Pinouts

TQ144 Pin	XC4005E	XC4006E
P1	GND	GND
P2	I/O, PGCK1 (A16)	I/O, PGCK1 (A16)
P3	I/O (A17)	I/O (A17)
P4	I/O	I/O
P5	I/O	I/O
P6	I/O, TDI	I/O, TDI
P7	I/O, TCK	I/O, TCK
P8	GND	GND
P9	I/O	I/O
P10	I/O	I/O
P11	I/O, TMS	I/O, TMS
P12	I/O	I/O
P13	I/O	I/O
P14	I/O	I/O
P15	I/O	I/O
P16	I/O	I/O
P17	GND	GND
P18	VCC	VCC
P19	I/O	I/O
P20	I/O	I/O
P21	I/O	I/O
P22	I/O	I/O
P23	I/O	I/O
P24	I/O	I/O
P25	I/O	I/O
P26	I/O	I/O
P27	GND	GND
P28	I/O	I/O
P29	I/O	I/O
P30	I/O	I/O
P31	I/O	I/O
P32	I/O	I/O
P33	I/O, SCGK2	I/O, SCGK2
P34	O (M1)	O (M1)
P35	GND	GND
P36	I (M0)	I (M0)
P37	VCC	VCC
P38	I (M2)	I (M2)
P39	I/O, PGCK2	I/O, PGCK2
P40	I/O (HDC)	I/O (HDC)
P41	I/O	I/O
P42	I/O	I/O
P43	I/O	I/O
P44	I/O ($\overline{\text{LDC}}$)	I/O ($\overline{\text{LDC}}$)
P45	GND	GND
P46	I/O	I/O
P47	I/O	I/O
P48	I/O	I/O
P49	I/O	I/O
P50	I/O	I/O
P51	I/O	I/O
P52	I/O	I/O
P53	I/O ($\overline{\text{INIT}}$)	I/O ($\overline{\text{INIT}}$)
P54	VCC	VCC
P55	GND	GND
P56	I/O	I/O
P57	I/O	I/O
P58	I/O	I/O
P59	I/O	I/O
P60	I/O	I/O
P61	I/O	I/O
P62	I/O	I/O
P63	I/O	I/O
P64	GND	GND
P65	I/O	I/O
P66	I/O	I/O
P67	I/O	I/O
P68	I/O	I/O
P69	I/O	I/O
P70	I/O, SGCK3	I/O, SGCK3
P71	GND	GND
P72	DONE	DONE
P73	VCC	VCC
P74	$\overline{\text{PROGRAM}}$	$\overline{\text{PROGRAM}}$
P75	I/O (D7)	I/O (D7)
P76	I/O, PGCK3	I/O, PGCK3
P77	I/O	I/O
P78	I/O	I/O
P79	I/O (D6)	I/O (D6)
P80	I/O	I/O
P81	GND	GND
P82	I/O	I/O
P83	I/O	I/O
P84	I/O (D5)	I/O (D5)
P85	I/O ($\overline{\text{CS0}}$)	I/O ($\overline{\text{CS0}}$)
P86	I/O	I/O
P87	I/O	I/O
P88	I/O (D4)	I/O (D4)
P89	I/O	I/O
P90	VCC	VCC
P91	GND	GND
P92	I/O (D3)	I/O (D3)
P93	I/O ($\overline{\text{RS}}$)	I/O ($\overline{\text{RS}}$)
P94	I/O	I/O

TQ144 Pin	XC4005E	XC4006E
P95	I/O	I/O
P96	I/O (D2)	I/O (D2)
P97	I/O	I/O
P98	I/O	I/O
P99	I/O	I/O
P100	GND	GND
P101	I/O (D1)	I/O (D1)
P102	I/O ($\overline{RCLK}$, RDY/$\overline{BUSY}$)	I/O ($\overline{RCLK}$, RDY/$\overline{BUSY}$)
P103	I/O	I/O
P104	I/O	I/O
P105	I/O (D0, DIN)	I/O (D0, DIN)
P106	I/O, SGCK4 (DOUT)	I/O, SGCK4 (DOUT)
P107	CCLK	CCLK
P108	VCC	VCC
P109	O, TDO	O, TDO
P110	GND	GND
P111	I/O (A0, $\overline{WS}$)	I/O (A0, $\overline{WS}$)
P112	I/O, PGCK4 (A1)	I/O, PGCK4 (A1)
P113	I/O	I/O
P114	I/O	I/O
P115	I/O (CS1, A2)	I/O (CS1, A2)
P116	I/O (A3)	I/O (A3)
P117	**N.C.**	**I/O**
P118	GND	GND
P119	I/O	I/O
P120	I/O	I/O
P121	I/O (A4)	I/O (A4)
P122	I/O (A5)	I/O (A5)
P123	I/O	I/O
P124	I/O	I/O
P125	I/O (A6)	I/O (A6)
P126	I/O (A7)	I/O (A7)
P127	GND	GND
P128	VCC	VCC
P129	I/O (A8)	I/O (A8)
P130	I/O (A9)	I/O (A9)
P131	I/O	I/O
P132	I/O	I/O
P133	I/O (A10)	I/O (A10)
P134	I/O (A11)	I/O (A11)
P135	I/O	I/O
P136	I/O	I/O
P137	GND	GND
P138	I/O (A12)	I/O (A12)
P139	I/O (A13)	I/O (A13)
P140	I/O	I/O
P141	I/O	I/O
P142	I/O (A14)	I/O (A14)
P143	I/O, SGCK1 (A15)	I/O, SGCK1 (A15)
P144	VCC	VCC

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Note: Shaded pins should be taken into account when designing PC boards, in case of future replacement by different devices.

PG156 Package Pinouts

PG156 Pin	XC4005E	XC4006E
T1	O, TDO	O, TDO
T2	I/O, SGCK4 (DOUT)	I/O, SGCK4 (DOUT)
T3	I/O (D1)	I/O (D1)
T4	I/O	I/O
T5	I/O	I/O
T6	I/O	I/O
T7	I/O ($\overline{RS}$)	I/O ($\overline{RS}$)
T8	I/O (D3)	I/O (D3)
T9	I/O	I/O
T10	I/O (D5)	I/O (D5)
T11	I/O	I/O
T12	**N.C.**	**I/O**
T13	I/O	I/O
T14	I/O (D6)	I/O (D6)
T15	I/O, PGCK3	I/O, PGCK3
T16	I/O (D7)	I/O (D7)
R1	I/O (A0, $\overline{WS}$)	I/O (A0, $\overline{WS}$)
R2	CCLK	CCLK
R3	I/O	I/O
R4	I/O	I/O
R5	**N.C.**	**I/O**
R6	I/O	I/O
R7	I/O	I/O
R8	VCC	VCC
R9	I/O (D4)	I/O (D4)
R10	I/O	I/O
R11	I/O	I/O
R12	**N.C.**	**I/O**
R13	I/O	I/O
R14	$\overline{PROGRAM}$	$\overline{PROGRAM}$
R15	DONE	DONE
R16	I/O, SGCK3	I/O, SGCK3
P1	I/O (CS1, A2)	I/O (CS1, A2)
P2	I/O, PGCK4 (A1)	I/O, PGCK4 (A1)
P3	VCC	VCC
P4	I/O (D0, DIN)	I/O (D0, DIN)
P5	I/O ($\overline{RCLK}$, RDY/$\overline{BUSY}$)	I/O ($\overline{RCLK}$, RDY/$\overline{BUSY}$)
P6	GND	GND
P7	I/O (D2)	I/O (D2)
P8	GND	GND
P9	I/O	I/O
P10	I/O ($\overline{CS0}$)	I/O ($\overline{CS0}$)
P11	GND	GND
P12	I/O	I/O
P13	VCC	VCC
P14	GND	GND
P15	I/O	I/O
P16	I/O	I/O
N1	I/O (A3)	I/O (A3)
N2	I/O	I/O
N3	GND	GND
N14	I/O	I/O
N15	I/O	I/O
N16	**N.C.**	**I/O**
M1	**N.C.**	**I/O**
M2	**N.C.**	**I/O**
M3	I/O	I/O
M14	I/O	I/O
M15	**N.C.**	**I/O**
M16	I/O	I/O
L1	I/O	I/O
L2	I/O	I/O
L3	GND	GND
L14	GND	GND
L15	I/O	I/O
L16	I/O	I/O
K1	I/O	I/O
K2	I/O (A5)	I/O (A5)
K3	I/O (A4)	I/O (A4)
K14	I/O	I/O
K15	I/O	I/O
K16	I/O	I/O
J1	I/O	I/O
J2	I/O (A6)	I/O (A6)
J3	I/O (A7)	I/O (A7)
J14	GND	GND
J15	I/O	I/O
J16	I/O	I/O
H1	I/O (A8)	I/O (A8)
H2	GND	GND
H3	VCC	VCC
H14	VCC	VCC
H15	I/O ($\overline{INIT}$)	I/O ($\overline{INIT}$)
H16	I/O	I/O
G1	I/O (A9)	I/O (A9)
G2	I/O	I/O
G3	I/O	I/O
G14	I/O	I/O
G15	I/O	I/O
G16	I/O	I/O
F1	I/O (A10)	I/O (A10)
F2	I/O (A11)	I/O (A11)
F3	GND	GND

PG156 Pin	XC4005E	XC4006E
F14	GND	GND
F15	I/O	I/O
F16	I/O	I/O
E1	I/O	I/O
E2	I/O	I/O
E3	I/O (A12)	I/O (A12)
E14	I/O	I/O
E15	**N.C.**	**I/O**
E16	I/O	I/O
D1	**N.C.**	**I/O**
D2	**N.C.**	**I/O**
D3	I/O	I/O
D14	I/O (HDC)	I/O (HDC)
D15	I/O	I/O
D16	**N.C.**	**I/O**
C1	I/O (A13)	I/O (A13)
C2	I/O	I/O
C3	VCC	VCC
C4	GND	GND
C5	I/O	I/O
C6	GND	GND
C7	I/O	I/O
C8	GND	GND
C9	I/O	I/O
C10	I/O	I/O
C11	GND	GND
C12	I/O	I/O
C13	GND	GND
C14	VCC	VCC
C15	I/O	I/O
C16	I/O ($\overline{LDC}$)	I/O ($\overline{LDC}$)
B1	I/O (A14)	I/O (A14)
B2	I/O, SGCK1 (A15)	I/O, SGCK1 (A15)
B3	I/O, PGCK1 (A16)	I/O, PGCK1 (A16)
B4	I/O, TDI	I/O, TDI
B5	I/O	I/O
B6	I/O	I/O
B7	I/O	I/O
B8	VCC	VCC
B9	I/O	I/O
B10	I/O	I/O
B11	I/O	I/O
B12	I/O	I/O
B13	I/O	I/O
B14	I/O, SCGK2	I/O, SCGK2
B15	I (M2)	I (M2)
B16	I/O, PGCK2	I/O, PGCK2
A1	I/O (A17)	I/O (A17)
A2	I/O	I/O
A3	I/O, TCK	I/O, TCK
A4	**N.C.**	**I/O**
A5	I/O, TMS	I/O, TMS
A6	I/O	I/O
A7	I/O	I/O
A8	I/O	I/O
A9	I/O	I/O
A10	I/O	I/O
A11	I/O	I/O
A12	**N.C.**	**I/O**
A13	I/O	I/O
A14	I/O	I/O
A15	O (M1)	O (M1)
A16	I (M0)	I (M0)

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Note: Shaded pins should be taken into account when designing PC boards, in case of future replacement by different devices.

Note: Viewed from the bottom side, the package pins start at the top row and go from the left edge to the right edge. Viewed from the top side, the pins start at the top row and go from the right edge to the left edge.

PQ160 Package Pinouts

PQ 160 Pin	XC4005E	XC4006E	XC4008E	XC4010E	XC4013E
P1	GND	GND	GND	GND	GND
P2	I/O, PGCK1 (A16)	I/O, PGCK1 (A16)	I/O, PGCK1 (A16)	I/O, PGCK1 (A16)	I/O, PGCK1 (A16)
P3	I/O (A17)	I/O (A17)	I/O (A17)	I/O (A17)	I/O (A17)
P4	I/O	I/O	I/O	I/O	I/O
P5	I/O	I/O	I/O	I/O	I/O
P6	I/O, TDI	I/O, TDI	I/O, TDI	I/O, TDI	I/O, TDI
P7	I/O, TCK	I/O, TCK	I/O, TCK	I/O, TCK	I/O, TCK
P8	**N.C.**	**I/O**	**I/O**	**I/O**	**I/O**
P9	**N.C.**	**I/O**	**I/O**	**I/O**	**I/O**
P10	GND	GND	GND	GND	GND
P11	I/O	I/O	I/O	I/O	I/O
P12	I/O	I/O	I/O	I/O	I/O
P13	I/O, TMS	I/O, TMS	I/O, TMS	I/O, TMS	I/O, TMS
P14	I/O	I/O	I/O	I/O	I/O
P15	I/O	I/O	I/O	I/O	I/O
P16	I/O	I/O	I/O	I/O	I/O
P17	I/O	I/O	I/O	I/O	I/O
P18	I/O	I/O	I/O	I/O	I/O
P19	GND	GND	GND	GND	GND
P20	VCC	VCC	VCC	VCC	VCC
P21	I/O	I/O	I/O	I/O	I/O
P22	I/O	I/O	I/O	I/O	I/O
P23	I/O	I/O	I/O	I/O	I/O
P24	I/O	I/O	I/O	I/O	I/O
P25	I/O	I/O	I/O	I/O	I/O
P26	I/O	I/O	I/O	I/O	I/O
P27	I/O	I/O	I/O	I/O	I/O
P28	I/O	I/O	I/O	I/O	I/O
P29	GND	GND	GND	GND	GND
P30	**N.C.**	**I/O**	**I/O**	**I/O**	**I/O**
P31	**N.C.**	**I/O**	**I/O**	**I/O**	**I/O**
P32	I/O	I/O	I/O	I/O	I/O
P33	I/O	I/O	I/O	I/O	I/O
P34	I/O	I/O	I/O	I/O	I/O
P35	I/O	I/O	I/O	I/O	I/O
P36	I/O	I/O	I/O	I/O	I/O
P37	I/O, SCGK2	I/O, SCGK2	I/O, SCGK2	I/O, SCGK2	I/O, SCGK2
P38	O (M1)	O (M1)	O (M1)	O (M1)	O (M1)
P39	GND	GND	GND	GND	GND
P40	I (M0)	I (M0)	I (M0)	I (M0)	I (M0)
P41	VCC	VCC	VCC	VCC	VCC
P42	I (M2)	I (M2)	I (M2)	I (M2)	I (M2)
P43	I/O, PGCK2	I/O, PGCK2	I/O, PGCK2	I/O, PGCK2	I/O, PGCK2
P44	I/O (HDC)	I/O (HDC)	I/O (HDC)	I/O (HDC)	I/O (HDC)
P45	I/O	I/O	I/O	I/O	I/O
P46	I/O	I/O	I/O	I/O	I/O
P47	I/O	I/O	I/O	I/O	I/O
P48	I/O ($\overline{LDC}$)	I/O ($\overline{LDC}$)	I/O ($\overline{LDC}$)	I/O ($\overline{LDC}$)	I/O ($\overline{LDC}$)
P49	**N.C.**	**I/O**	**I/O**	**I/O**	**I/O**
P50	**N.C.**	**I/O**	**I/O**	**I/O**	**I/O**
P51	GND	GND	GND	GND	GND
P52	I/O	I/O	I/O	I/O	I/O
P53	I/O	I/O	I/O	I/O	I/O
P54	I/O	I/O	I/O	I/O	I/O
P55	I/O	I/O	I/O	I/O	I/O
P56	I/O	I/O	I/O	I/O	I/O
P57	I/O	I/O	I/O	I/O	I/O
P58	I/O	I/O	I/O	I/O	I/O
P59	I/O ($\overline{INIT}$)	I/O ($\overline{INIT}$)	I/O ($\overline{INIT}$)	I/O ($\overline{INIT}$)	I/O ($\overline{INIT}$)
P60	VCC	VCC	VCC	VCC	VCC
P61	GND	GND	GND	GND	GND
P62	I/O	I/O	I/O	I/O	I/O
P63	I/O	I/O	I/O	I/O	I/O
P64	I/O	I/O	I/O	I/O	I/O
P65	I/O	I/O	I/O	I/O	I/O
P66	I/O	I/O	I/O	I/O	I/O
P67	I/O	I/O	I/O	I/O	I/O
P68	I/O	I/O	I/O	I/O	I/O
P69	I/O	I/O	I/O	I/O	I/O
P70	GND	GND	GND	GND	GND
P71	**N.C.**	**I/O**	**I/O**	**I/O**	**I/O**
P72	**N.C.**	**I/O**	**I/O**	**I/O**	**I/O**
P73	I/O	I/O	I/O	I/O	I/O
P74	I/O	I/O	I/O	I/O	I/O
P75	I/O	I/O	I/O	I/O	I/O
P76	I/O	I/O	I/O	I/O	I/O
P77	I/O	I/O	I/O	I/O	I/O
P78	I/O, SGCK3	I/O, SGCK3	I/O, SGCK3	I/O, SGCK3	I/O, SGCK3
P79	GND	GND	GND	GND	GND
P80	DONE	DONE	DONE	DONE	DONE
P81	VCC	VCC	VCC	VCC	VCC
P82	$\overline{PROGRAM}$	$\overline{PROGRAM}$	$\overline{PROGRAM}$	$\overline{PROGRAM}$	$\overline{PROGRAM}$
P83	I/O (D7)	I/O (D7)	I/O (D7)	I/O (D7)	I/O (D7)
P84	I/O, PGCK3	I/O, PGCK3	I/O, PGCK3	I/O, PGCK3	I/O, PGCK3
P85	I/O	I/O	I/O	I/O	I/O
P86	I/O	I/O	I/O	I/O	I/O
P87	I/O (D6)	I/O (D6)	I/O (D6)	I/O (D6)	I/O (D6)
P88	I/O	I/O	I/O	I/O	I/O
P89	**N.C.**	**I/O**	**I/O**	**I/O**	**I/O**
P90	**N.C.**	**I/O**	**I/O**	**I/O**	**I/O**
P91	GND	GND	GND	GND	GND
P92	I/O	I/O	I/O	I/O	I/O
P93	I/O	I/O	I/O	I/O	I/O
P94	I/O (D5)	I/O (D5)	I/O (D5)	I/O (D5)	I/O (D5)
P95	I/O ($\overline{CS0}$)	I/O ($\overline{CS0}$)	I/O ($\overline{CS0}$)	I/O ($\overline{CS0}$)	I/O ($\overline{CS0}$)

PQ 160 Pin	XC4005E	XC4006E	XC4008E	XC4010E	XC4013E
P96	I/O	I/O	I/O	I/O	I/O
P97	I/O	I/O	I/O	I/O	I/O
P98	I/O (D4)	I/O (D4)	I/O (D4)	I/O (D4)	I/O (D4)
P99	I/O	I/O	I/O	I/O	I/O
P100	VCC	VCC	VCC	VCC	VCC
P101	GND	GND	GND	GND	GND
P102	I/O (D3)	I/O (D3)	I/O (D3)	I/O (D3)	I/O (D3)
P103	I/O ($\overline{RS}$)	I/O ($\overline{RS}$)	I/O ($\overline{RS}$)	I/O ($\overline{RS}$)	I/O ($\overline{RS}$)
P104	I/O	I/O	I/O	I/O	I/O
P105	I/O	I/O	I/O	I/O	I/O
P106	I/O (D2)	I/O (D2)	I/O (D2)	I/O (D2)	I/O (D2)
P107	I/O	I/O	I/O	I/O	I/O
P108	I/O	I/O	I/O	I/O	I/O
P109	I/O	I/O	I/O	I/O	I/O
P110	GND	GND	GND	GND	GND
P111	**N.C.**	**I/O**	**I/O**	**I/O**	**I/O**
P112	**N.C.**	**I/O**	**I/O**	**I/O**	**I/O**
P113	I/O (D1)	I/O (D1)	I/O (D1)	I/O (D1)	I/O (D1)
P114	I/O ($\overline{RCLK}$, RDY/ $\overline{BUSY}$)	I/O ($\overline{RCLK}$, RDY/ $\overline{BUSY}$)	I/O ($\overline{RCLK}$, RDY/ $\overline{BUSY}$)	I/O ($\overline{RCLK}$, RDY/ $\overline{BUSY}$)	I/O ($\overline{RCLK}$, RDY/ $\overline{BUSY}$)
P115	I/O	I/O	I/O	I/O	I/O
P116	I/O	I/O	I/O	I/O	I/O
P117	I/O (D0, DIN)	I/O (D0, DIN)	I/O (D0, DIN)	I/O (D0, DIN)	I/O (D0. DIN)
P118	I/O, SGCK4 (DOUT)	I/O, SGCK4 (DOUT)	I/O, SGCK4 (DOUT)	I/O, SGCK4 (DOUT)	I/O, SGCK4 (DOUT)
P119	CCLK	CCLK	CCLK	CCLK	CCLK
P120	VCC	VCC	VCC	VCC	VCC
P121	O, TDO	O, TDO	O, TDO	O, TDO	O, TDO
P122	GND	GND	GND	GND	GND
P123	I/O (A0, $\overline{WS}$)	I/O (A0, $\overline{WS}$)	I/O (A0, $\overline{WS}$)	I/O (A0. $\overline{WS}$)	I/O (A0, $\overline{WS}$)
P124	I/O, PGCK4 (A1)	I/O, PGCK4 (A1)	I/O, PGCK4 (A1)	I/O, PGCK4 (A1)	I/O, PGCK4 (A1)
P125	I/O	I/O	I/O	I/O	I/O
P126	I/O	I/O	I/O	I/O	I/O
P127	I/O (CS1, A2)	I/O (CS1, A2)	I/O (CS1, A2)	I/O (CS1, A2)	I/O (CS1, A2)
P128	I/O (A3)	I/O (A3)	I/O (A3)	I/O (A3)	I/O (A3)
P129	**N.C.**	**I/O**	**I/O**	**I/O**	**I/O**
P130	**N.C.**	**I/O**	**I/O**	**I/O**	**I/O**
P131	GND	GND	GND	GND	GND
P132	I/O	I/O	I/O	I/O	I/O
P133	I/O	I/O	I/O	I/O	I/O
P134	I/O (A4)	I/O (A4)	I/O (A4)	I/O (A4)	I/O (A4)
P135	I/O (A5)	I/O (A5)	I/O (A5)	I/O (A5)	I/O (A5)
P136	**N.C.**	**N.C.**	**I/O**	**I/O**	**I/O**
P137	I/O	I/O	I/O	I/O	I/O
P138	I/O	I/O	I/O	I/O	I/O
P139	I/O (A6)	I/O (A6)	I/O (A6)	I/O (A6)	I/O (A6)
P140	I/O (A7)	I/O (A7)	I/O (A7)	I/O (A7)	I/O (A7)
P141	GND	GND	GND	GND	GND
P142	VCC	VCC	VCC	VCC	VCC
P143	I/O (A8)	I/O (A8)	I/O (A8)	I/O (A8)	I/O (A8)
P144	I/O (A9)	I/O (A9)	I/O (A9)	I/O (A9)	I/O (A9)
P145	I/O	I/O	I/O	I/O	I/O
P146	I/O	I/O	I/O	I/O	I/O
P147	I/O (A10)	I/O (A10)	I/O (A10)	I/O (A10)	I/O (A10)
P148	I/O (A11)	I/O (A11)	I/O (A11)	I/O (A11)	I/O (A11)
P149	I/O	I/O	I/O	I/O	I/O
P150	I/O	I/O	I/O	I/O	I/O
P151	GND	GND	GND	GND	GND
P152	**N.C.**	**I/O**	**I/O**	**I/O**	**I/O**
P153	**N.C.**	**I/O**	**I/O**	**I/O**	**I/O**
P154	I/O (A12)	I/O (A12)	I/O (A12)	I/O (A12)	I/O (A12)
P155	I/O (A13)	I/O (A13)	I/O (A13)	I/O (A13)	I/O (A13)
P156	I/O	I/O	I/O	I/O	I/O
P157	I/O	I/O	I/O	I/O	I/O
P158	I/O (A14)	I/O (A14)	I/O (A14)	I/O (A14)	I/O (A14)
P159	I/O, SGCK1 (A15)	I/O, SGCK1 (A15)	I/O, SGCK1 (A15)	I/O, SGCK1 (A15)	I/O, SGCK1 (A15)
P160	VCC	VCC	VCC	VCC	VCC

2/28/96

Note: Shaded pins should be taken into account when designing PC boards, in case of future replacement by different devices.

TQ176 Package Pinouts

TQ176 Pin	XC4010L
P1	GND
P2	I/O, PGCK1 (A16)
P3	I/O (A17)
P4	I/O
P5	I/O
P6	I/O, TDI
P7	I/O, TCK
P8	I/O
P9	I/O
P10	GND
P11	I/O
P12	I/O
P13	I/O, TMS
P14	I/O
P15	I/O
P16	I/O
P17	I/O
P18	I/O
P19	I/O
P20	I/O
P21	GND
P22	VCC
P23	I/O
P24	I/O
P25	I/O
P26	I/O
P27	I/O
P28	I/O
P29	I/O
P30	I/O
P31	I/O
P32	I/O
P33	GND
P34	I/O
P35	I/O
P36	I/O
P37	I/O
P38	I/O
P39	I/O
P40	I/O
P41	I/O, SCGK2
P42	O (M1)
P43	GND
P44	I (M0)
P45	VCC
P46	I (M2)
P47	I/O, PGCK2
P48	I/O (HDC)
P49	I/O
P50	I/O
P51	I/O
P52	I/O ($\overline{\text{LDC}}$)
P53	I/O
P54	I/O
P55	GND
P56	I/O
P57	I/O
P58	I/O
P59	I/O
P60	I/O
P61	I/O
P62	I/O
P63	I/O
P64	I/O
P65	I/O ($\overline{\text{INIT}}$)
P66	VCC
P67	GND
P68	I/O
P69	I/O
P70	I/O
P71	I/O
P72	I/O
P73	I/O
P74	I/O
P75	I/O
P76	I/O
P77	I/O
P78	GND
P79	I/O
P80	I/O
P81	I/O
P82	I/O
P83	I/O
P84	I/O
P85	I/O
P86	I/O, SGCK3
P87	GND
P88	DONE
P89	VCC
P90	$\overline{\text{PROGRAM}}$
P91	I/O (D7)
P92	I/O, PGCK3
P93	I/O
P94	I/O

TQ176 Pin	XC4010L
P95	I/O (D6)
P96	I/O
P97	I/O
P98	I/O
P99	GND
P100	I/O
P101	I/O
P102	I/O (D5)
P103	I/O ($\overline{CS0}$)
P104	I/O
P105	I/O
P106	I/O
P107	I/O
P108	I/O (D4)
P109	I/O
P110	VCC
P111	GND
P112	I/O (D3)
P113	I/O ($\overline{RS}$)
P114	I/O
P115	I/O
P116	I/O
P117	I/O
P118	I/O (D2)
P119	I/O
P120	I/O
P121	I/O
P122	GND
P123	I/O
P124	I/O
P125	I/O (D1)
P126	I/O ($\overline{RCLK}$, RDY/$\overline{BUSY}$)
P127	I/O
P128	I/O
P129	I/O (D0, DIN)
P130	I/O, SGCK4 (DOUT)
P131	CCLK
P132	VCC
P133	O, TDO
P134	GND
P135	I/O (A0, $\overline{WS}$)
P136	I/O, PGCK4 (A1)
P137	I/O
P138	I/O
P139	I/O (CS1, A2)
P140	I/O (A3)
P141	I/O
P142	I/O
P143	GND
P144	I/O
P145	I/O
P146	I/O (A4)
P147	I/O (A5)
P148	I/O
P149	I/O
P150	I/O
P151	I/O
P152	I/O (A6)
P153	I/O (A7)
P154	GND
P155	VCC
P156	I/O (A8)
P157	I/O (A9)
P158	I/O
P159	I/O
P160	I/O
P161	I/O
P162	I/O (A10)
P163	I/O (A11)
P164	I/O
P165	I/O
P166	GND
P167	I/O
P168	I/O
P169	I/O
P170	I/O (A12)
P171	I/O (A13)
P172	I/O
P173	I/O
P174	I/O (A14)
P175	I/O, SGCK1 (A15)
P176	VCC

3/15/96

PG191 Package Pinouts (see PG223)

The PG191 package pinout has been combined with the PG223 in a single table, because of their physical compatibility. The PG191 has the same dimensions as the PG223, but has 32 fewer pins on the inner ring.

PQ208, HQ208 Package Pinouts

PQ 208 Pin	XC 4005 E/L	XC 4006 E	XC 4008 E	XC 4010 E/L	XC 4013 E/L	XC 4020 E	XC 4028 EX/XL
P1	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.
P2	GND	GND	GND	GND	GND	GND	GND
P3	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.
P4	I/O, PGCK1 (A16)	I/O, PGCK1 (A16)	I/O, PGCK1 (A16)	I/O, PGCK1 (A16)	I/O, PGCK1 (A16)	I/O, PGCK1 (A16)	I/O, GCK1 (A16)
P5	I/O (A17)	I/O (A17)	I/O (A17)	I/O (A17)	I/O (A17)	I/O (A17)	I/O (A17)
P6	I/O	I/O	I/O	I/O	I/O	I/O	I/O
P7	I/O	I/O	I/O	I/O	I/O	I/O	I/O
P8	I/O, TDI	I/O, TDI	I/O, TDI	I/O, TDI	I/O, TDI	I/O, TDI	I/O, TDI
P9	I/O, TCK	I/O, TCK	I/O, TCK	I/O, TCK	I/O, TCK	I/O, TCK	I/O, TCK
P10	**N.C.**	**I/O**	**I/O**	**I/O**	**I/O**	**I/O**	**I/O**
P11	**N.C.**	**I/O**	**I/O**	**I/O**	**I/O**	**I/O**	**I/O**
P12	**N.C.**	**N.C.**	**N.C.**	**I/O**	**I/O**	**I/O**	**I/O**
P13	**N.C.**	**N.C.**	**N.C.**	**I/O**	**I/O**	**I/O**	**I/O**
P14	GND	GND	GND	GND	GND	GND	GND
P15	I/O	I/O	I/O	I/O	I/O	I/O	I/O, FCLK1
P16	I/O	I/O	I/O	I/O	I/O	I/O	I/O
P17	I/O, TMS	I/O, TMS	I/O, TMS	I/O, TMS	I/O, TMS	I/O, TMS	I/O, TMS
P18	I/O	I/O	I/O	I/O	I/O	I/O	I/O
P19	**N.C.**	**N.C.**	**I/O**	**I/O**	**I/O**	**I/O**	**I/O**
P20	**N.C.**	**N.C.**	**I/O**	**I/O**	**I/O**	**I/O**	**I/O**
P21	I/O	I/O	I/O	I/O	I/O	I/O	I/O
P22	I/O	I/O	I/O	I/O	I/O	I/O	I/O
P23	I/O	I/O	I/O	I/O	I/O	I/O	I/O
P24	I/O	I/O	I/O	I/O	I/O	I/O	I/O
P25	GND	GND	GND	GND	GND	GND	GND
P26	VCC	VCC	VCC	VCC	VCC	VCC	VCC
P27	I/O	I/O	I/O	I/O	I/O	I/O	I/O
P28	I/O	I/O	I/O	I/O	I/O	I/O	I/O
P29	I/O	I/O	I/O	I/O	I/O	I/O	I/O
P30	I/O	I/O	I/O	I/O	I/O	I/O	I/O
P31	**N.C.**	**N.C.**	**I/O**	**I/O**	**I/O**	**I/O**	**I/O**
P32	**N.C.**	**N.C.**	**I/O**	**I/O**	**I/O**	**I/O**	**I/O**
P33	I/O	I/O	I/O	I/O	I/O	I/O	I/O
P34	I/O	I/O	I/O	I/O	I/O	I/O	I/O
P35	I/O	I/O	I/O	I/O	I/O	I/O	I/O
P36	I/O	I/O	I/O	I/O	I/O	I/O	I/O, FCLK2
P37	GND	GND	GND	GND	GND	GND	GND
P38	**N.C.**	**N.C.**	**N.C.**	**I/O**	**I/O**	**I/O**	**I/O**
P39	**N.C.**	**N.C.**	**N.C.**	**I/O**	**I/O**	**I/O**	**I/O**
P40	**N.C.**	**I/O**	**I/O**	**I/O**	**I/O**	**I/O**	**I/O**
P41	**N.C.**	**I/O**	**I/O**	**I/O**	**I/O**	**I/O**	**I/O**
P42	I/O	I/O	I/O	I/O	I/O	I/O	I/O
P43	I/O	I/O	I/O	I/O	I/O	I/O	I/O
P44	I/O	I/O	I/O	I/O	I/O	I/O	I/O

PQ 208 Pin	XC 4005 E/L	XC 4006 E	XC 4008 E	XC 4010 E/L	XC 4013 E/L	XC 4020 E	XC 4028 EX/XL
P45	I/O	I/O	I/O	I/O	I/O	I/O	I/O
P46	I/O	I/O	I/O	I/O	I/O	I/O	I/O
P47	I/O, SGCK2	I/O, SGCK2	I/O, SGCK2	I/O, SGCK2	I/O, SGCK2	I/O, SGCK2	I/O, GCK2
P48	O (M1)	O (M1)	O (M1)	O (M1)	O (M1)	O (M1)	O (M1)
P49	GND	GND	GND	GND	GND	GND	GND
P50	I (M0)	I (M0)	I (M0)	I (M0)	I (M0)	I (M0)	I (M0)
P51	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.
P52	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.
P53	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.
P54	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.
P55	VCC	VCC	VCC	VCC	VCC	VCC	VCC
P56	I (M2)	I (M2)	I (M2)	I (M2)	I (M2)	I (M2)	I (M2)
P57	I/O, PGCK2	I/O, PGCK2	I/O, PGCK2	I/O, PGCK2	I/O, PGCK2	I/O, PGCK2	I/O, GCK3
P58	I/O (HDC)	I/O (HDC)	I/O (HDC)	I/O (HDC)	I/O (HDC)	I/O (HDC)	I/O (HDC)
P59	I/O	I/O	I/O	I/O	I/O	I/O	I/O
P60	I/O	I/O	I/O	I/O	I/O	I/O	I/O
P61	I/O	I/O	I/O	I/O	I/O	I/O	I/O
P62	I/O (LDC)	I/O (LDC)	I/O (LDC)	I/O (LDC)	I/O (LDC)	I/O (LDC)	I/O (LDC)
P63	**N.C.**	**I/O**	**I/O**	**I/O**	**I/O**	**I/O**	**I/O**
P64	**N.C.**	**I/O**	**I/O**	**I/O**	**I/O**	**I/O**	**I/O**
P65	**N.C.**	**N.C.**	**N.C.**	**I/O**	**I/O**	**I/O**	**I/O**
P66	**N.C.**	**N.C.**	**N.C.**	**I/O**	**I/O**	**I/O**	**I/O**
P67	GND	GND	GND	GND	GND	GND	GND
P68	I/O	I/O	I/O	I/O	I/O	I/O	I/O
P69	I/O	I/O	I/O	I/O	I/O	I/O	I/O
P70	I/O	I/O	I/O	I/O	I/O	I/O	I/O
P71	I/O	I/O	I/O	I/O	I/O	I/O	I/O
P72	**N.C.**	**N.C.**	**I/O**	**I/O**	**I/O**	**I/O**	**I/O**
P73	**N.C.**	**N.C.**	**I/O**	**I/O**	**I/O**	**I/O**	**I/O**
P74	I/O	I/O	I/O	I/O	I/O	I/O	I/O
P75	I/O	I/O	I/O	I/O	I/O	I/O	I/O
P76	I/O	I/O	I/O	I/O	I/O	I/O	I/O
P77	I/O (INIT)	I/O (INIT)	I/O (INIT)	I/O (INIT)	I/O (INIT)	I/O (INIT)	I/O (INIT)
P78	VCC	VCC	VCC	VCC	VCC	VCC	VCC
P79	GND	GND	GND	GND	GND	GND	GND
P80	I/O	I/O	I/O	I/O	I/O	I/O	I/O
P81	I/O	I/O	I/O	I/O	I/O	I/O	I/O
P82	I/O	I/O	I/O	I/O	I/O	I/O	I/O
P83	I/O	I/O	I/O	I/O	I/O	I/O	I/O
P84	**N.C.**	**N.C.**	**I/O**	**I/O**	**I/O**	**I/O**	**I/O**
P85	**N.C.**	**N.C.**	**I/O**	**I/O**	**I/O**	**I/O**	**I/O**
P86	I/O	I/O	I/O	I/O	I/O	I/O	I/O
P87	I/O	I/O	I/O	I/O	I/O	I/O	I/O
P88	I/O	I/O	I/O	I/O	I/O	I/O	I/O
P89	I/O	I/O	I/O	I/O	I/O	I/O	I/O
P90	GND	GND	GND	GND	GND	GND	GND
P91	**N.C.**	**N.C.**	**N.C.**	**I/O**	**I/O**	**I/O**	**I/O**

PQ 208 Pin	XC 4005 E/L	XC 4006 E	XC 4008 E	XC 4010 E/L	XC 4013 E/L	XC 4020 E	XC 4028 EX/XL
P92	N.C.	N.C.	N.C.	I/O	I/O	I/O	I/O
P93	N.C.	I/O	I/O	I/O	I/O	I/O	I/O
P94	N.C.	I/O	I/O	I/O	I/O	I/O	I/O
P95	I/O	I/O	I/O	I/O	I/O	I/O	I/O
P96	I/O	I/O	I/O	I/O	I/O	I/O	I/O
P97	I/O	I/O	I/O	I/O	I/O	I/O	I/O
P98	I/O	I/O	I/O	I/O	I/O	I/O	I/O
P99	I/O	I/O	I/O	I/O	I/O	I/O	I/O
P100	I/O, SGCK3	I/O, SGCK3	I/O, SGCK3	I/O, SGCK3	I/O, SGCK3	I/O, SGCK3	I/O, GCK4
P101	GND	GND	GND	GND	GND	GND	GND
P102	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.
P103	DONE	DONE	DONE	DONE	DONE	DONE	DONE
P104	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.
P105	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.
P106	VCC	VCC	VCC	VCC	VCC	VCC	VCC
P107	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.
P108	PROGRAM	PROGRAM	PROGRAM	PROGRAM	PROGRAM	PROGRAM	PROGRAM
P109	I/O (D7)	I/O (D7)	I/O (D7)	I/O (D7)	I/O (D7)	I/O (D7)	I/O (D7)
P110	I/O, PGCK3	I/O, PGCK3	I/O, PGCK3	I/O, PGCK3	I/O, PGCK3	I/O, PGCK3	I/O, GCK5
P111	I/O	I/O	I/O	I/O	I/O	I/O	I/O
P112	I/O	I/O	I/O	I/O	I/O	I/O	I/O
P113	I/O (D6)	I/O (D6)	I/O (D6)	I/O (D6)	I/O (D6)	I/O (D6)	I/O (D6)
P114	I/O	I/O	I/O	I/O	I/O	I/O	I/O
P115	N.C.	I/O	I/O	I/O	I/O	I/O	I/O
P116	N.C.	I/O	I/O	I/O	I/O	I/O	I/O
P117	N.C.	N.C.	N.C.	I/O	I/O	I/O	I/O
P118	N.C.	N.C.	N.C.	I/O	I/O	I/O	I/O
P119	GND	GND	GND	GND	GND	GND	GND
P120	I/O	I/O	I/O	I/O	I/O	I/O	I/O, FCLK3
P121	I/O	I/O	I/O	I/O	I/O	I/O	I/O
P122	I/O (D5)	I/O (D5)	I/O (D5)	I/O (D5)	I/O (D5)	I/O (D5)	I/O (D5)
P123	I/O (CS0)	I/O (CS0)	I/O (CS0)	I/O (CS0)	I/O (CS0)	I/O (CS0)	I/O (CS0)
P124	N.C.	N.C.	I/O	I/O	I/O	I/O	I/O
P125	N.C.	N.C.	I/O	I/O	I/O	I/O	I/O
P126	I/O	I/O	I/O	I/O	I/O	I/O	I/O
P127	I/O	I/O	I/O	I/O	I/O	I/O	I/O
P128	I/O (D4)	I/O (D4)	I/O (D4)	I/O (D4)	I/O (D4)	I/O (D4)	I/O (D4)
P129	I/O	I/O	I/O	I/O	I/O	I/O	I/O
P130	VCC	VCC	VCC	VCC	VCC	VCC	VCC
P131	GND	GND	GND	GND	GND	GND	GND
P132	I/O (D3)	I/O (D3)	I/O (D3)	I/O (D3)	I/O (D3)	I/O (D3)	I/O (D3)
P133	I/O (RS)	I/O (RS)	I/O (RS)	I/O (RS)	I/O (RS)	I/O (RS)	I/O (RS)
P134	I/O	I/O	I/O	I/O	I/O	I/O	I/O
P135	I/O	I/O	I/O	I/O	I/O	I/O	I/O
P136	N.C.	N.C.	I/O	I/O	I/O	I/O	I/O
P137	N.C.	N.C.	I/O	I/O	I/O	I/O	I/O

PQ 208 Pin	XC 4005 E/L	XC 4006 E	XC 4008 E	XC 4010 E/L	XC 4013 E/L	XC 4020 E	XC 4028 EX/XL
P138	I/O (D2)	I/O (D2)	I/O (D2)	I/O (D2)	I/O (D2)	I/O (D2)	I/O (D2)
P139	I/O	I/O	I/O	I/O	I/O	I/O	I/O
P140	I/O	I/O	I/O	I/O	I/O	I/O	I/O
P141	I/O	I/O	I/O	I/O	I/O	I/O	I/O, FCLK4
P142	GND	GND	GND	GND	GND	GND	GND
P143	N.C.	N.C.	N.C.	I/O	I/O	I/O	I/O
P144	N.C.	N.C.	N.C.	I/O	I/O	I/O	I/O
P145	N.C.	I/O	I/O	I/O	I/O	I/O	I/O
P146	N.C.	I/O	I/O	I/O	I/O	I/O	I/O
P147	I/O (D1)	I/O (D1)	I/O (D1)	I/O (D1)	I/O (D1)	I/O (D1)	I/O (D1)
P148	I/O (RCLK, RDY/ BUSY)	I/O (RCLK, RDY/ BUSY)	I/O (RCLK, RDY/ BUSY)	I/O (RCLK, RDY/ BUSY)	I/O (RCLK, RDY/ BUSY)	I/O (RCLK, RDY/ BUSY)	I/O (RCLK, RDY/ BUSY)
P149	I/O	I/O	I/O	I/O	I/O	I/O	I/O
P150	I/O	I/O	I/O	I/O	I/O	I/O	I/O
P151	I/O (D0, DIN)	I/O (D0, DIN)	I/O (D0, DIN)	I/O (D0, DIN)	I/O (D0, DIN)	I/O (D0, DIN)	I/O (D0, DIN)
P152	I/O, SGCK (DOUT)	I/O, SGCK4 (DOUT)	I/O, SGCK4 (DOUT)	I/O, SGCK4 (DOUT)	I/O, SGCK4 (DOUT)	I/O, SGCK4 (DOUT)	I/O, GCK6 (DOUT)
P153	CCLK	CCLK	CCLK	CCLK	CCLK	CCLK	CCLK
P154	VCC	VCC	VCC	VCC	VCC	VCC	VCC
P155	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.
P156	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.
P157	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.
P158	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.
P159	O, TDO	O, TDO	O, TDO	O, TDO	O, TDO	O, TDO	O, TDO
P160	GND	GND	GND	GND	GND	GND	GND
P161	I/O (A0, WS)	I/O (A0, WS)	I/O (A0, WS)	I/O (A0. WS)	I/O (A0, WS)	I/O (A0, WS)	I/O (A0, WS)
P162	I/O, PGCK4 (A1)	I/O, PGCK4 (A1)	I/O, PGCK4 (A1)	I/O. PGCK4 (A1)	I/O, PGCK4 (A1)	I/O, PGCK4 (A1)	I/O, GCK7 (A1)
P163	I/O	I/O	I/O	I/O	I/O	I/O	I/O
P164	I/O	I/O	I/O	I/O	I/O	I/O	I/O
P165	I/O (CS1, A2)	I/O (CS1, A2)	I/O (CS1, A2)	I/O (CS1. A2)	I/O (CS1, A2)	I/O (CS1, A2)	I/O (CS1, A2)
P166	I/O (A3)	I/O (A3)	I/O (A3)	I/O (A3)	I/O (A3)	I/O (A3)	I/O (A3)
P167	N.C.	I/O	I/O	I/O	I/O	I/O	I/O
P168	N.C.	I/O	I/O	I/O	I/O	I/O	I/O
P169	N.C.	N.C.	N.C.	I/O	I/O	I/O	I/O
P170	N.C.	N.C.	N.C.	I/O	I/O	I/O	I/O
P171	GND	GND	GND	GND	GND	GND	GND
P172	I/O	I/O	I/O	I/O	I/O	I/O	I/O
P173	I/O	I/O	I/O	I/O	I/O	I/O	I/O
P174	I/O (A4)	I/O (A4)	I/O (A4)	I/O (A4)	I/O (A4)	I/O (A4)	I/O (A4)
P175	I/O (A5)	I/O (A5)	I/O (A5)	I/O (A5)	I/O (A5)	I/O (A5)	I/O (A5)
P176	N.C.	N.C.	I/O	I/O	I/O	I/O	I/O
P177	N.C.	N.C.	I/O	I/O	I/O	I/O	I/O

PQ 208 Pin	XC 4005 E/L	XC 4006 E	XC 4008 E	XC 4010 E/L	XC 4013 E/L	XC 4020 E	XC 4028 EX/XL
P178	I/O	I/O	I/O	I/O	I/O	I/O	I/O (A21)
P179	I/O	I/O	I/O	I/O	I/O	I/O	I/O (A20)
P180	I/O (A6)	I/O (A6)	I/O (A6)	I/O (A6)	I/O (A6)	I/O (A6)	I/O (A6)
P181	I/O (A7)	I/O (A7)	I/O (A7)	I/O (A7)	I/O (A7)	I/O (A7)	I/O (A7)
P182	GND	GND	GND	GND	GND	GND	GND
P183	VCC	VCC	VCC	VCC	VCC	VCC	VCC
P184	I/O (A8)	I/O (A8)	I/O (A8)	I/O (A8)	I/O (A8)	I/O (A8)	I/O (A8)
P185	I/O (A9)	I/O (A9)	I/O (A9)	I/O (A9)	I/O (A9)	I/O (A9)	I/O (A9)
P186	I/O	I/O	I/O	I/O	I/O	I/O	I/O (A19)
P187	I/O	I/O	I/O	I/O	I/O	I/O	I/O (A18)
P188	N.C.	N.C.	I/O	I/O	I/O	I/O	I/O
P189	N.C.	N.C.	I/O	I/O	I/O	I/O	I/O
P190	I/O (A10)	I/O (A10)	I/O (A10)	I/O (A10)	I/O (A10)	I/O (A10)	I/O (A10)
P191	I/O (A11)	I/O (A11)	I/O (A11)	I/O (A11)	I/O (A11)	I/O (A11)	I/O (A11)
P192	I/O	I/O	I/O	I/O	I/O	I/O	I/O
P193	I/O	I/O	I/O	I/O	I/O	I/O	I/O
P194	GND	GND	GND	GND	GND	GND	GND
P195	N.C.	N.C.	N.C.	I/O	I/O	I/O	I/O

PQ 208 Pin	XC 4005 E/L	XC 4006 E	XC 4008 E	XC 4010 E/L	XC 4013 E/L	XC 4020 E	XC 4028 EX/XL
P196	N.C.	N.C.	N.C.	I/O	I/O	I/O	I/O
P197	N.C.	I/O	I/O	I/O	I/O	I/O	I/O
P198	N.C.	I/O	I/O	I/O	I/O	I/O	I/O
P199	I/O (A12)	I/O (A12)	I/O (A12)	I/O (A12)	I/O (A12)	I/O (A12)	I/O (A12)
P200	I/O (A13)	I/O (A13)	I/O (A13)	I/O (A13)	I/O (A13)	I/O (A13)	I/O (A13)
P201	I/O	I/O	I/O	I/O	I/O	I/O	I/O
P202	I/O	I/O	I/O	I/O	I/O	I/O	I/O
P203	I/O (A14)	I/O (A14)	I/O (A14)	I/O (A14)	I/O (A14)	I/O (A14)	I/O (A14)
P204	I/O, SGCK1 (A15)	I/O, SGCK1 (A15)	I/O, SGCK1 (A15)	I/O, SGCK1 (A15)	I/O, SGCK1 (A15)	I/O, SGCK1 (A15)	I/O, GCK8 (A15)
P205	VCC	VCC	VCC	VCC	VCC	VCC	VCC
P206	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.
P207	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.
P208	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.

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Note: Shaded pins should be taken into account when designing PC boards, in case of future replacement by different devices.

PG223 and PG191 Package Pinouts

These two packages have been combined into a single table because of their physical compatibility. The PG191 has the same dimensions as the PG223, but has 32 fewer pins on the inner ring.

PG 223 Pin	PG 191 Pin	XC4008E PG191	XC4010E PG191	XC4013E PG223	XC4020E PG223	XC4025E PG223
V1	V1	CCLK	CCLK	CCLK	CCLK	CCLK
V2	V2	I/O (RCLK, RDY/ BUSY)	I/O (RCLK, RDY/ BUSY)	I/O (RCLK, RDY/ BUSY)	I/O (RCLK, RDY/ BUSY)	I/O (RCLK, RDY/ BUSY)
V3	V3	I/O (D1)	I/O (D1)	I/O (D1)	I/O (D1)	I/O (D1)
V4	V4	N.C.	I/O	I/O	I/O	I/O
V5	V5	N.C.	I/O	I/O	I/O	I/O
V6	V6	I/O	I/O	I/O	I/O	I/O
V7	V7	I/O (D2)	I/O (D2)	I/O (D2)	I/O (D2)	I/O (D2)
V8	V8	I/O	I/O	I/O	I/O	I/O
V9	V9	I/O	I/O	I/O	I/O	I/O
V10	V10	I/O	I/O	I/O	I/O	I/O
V11	V11	I/O	I/O	I/O	I/O	I/O
V12	V12	I/O (CS0)	I/O (CS0)	I/O (CS0)	I/O (CS0)	I/O (CS0)
V13	V13	I/O	I/O	I/O	I/O	I/O
V14	V14	N.C.	I/O	I/O	I/O	I/O
V15	V15	N.C.	I/O	I/O	I/O	I/O
V16	V16	I/O	I/O	I/O	I/O	I/O
V17	V17	I/O (D6)	I/O (D6)	I/O (D6)	I/O (D6)	I/O (D6)
V18	V18	PRO-GRAM	PRO-GRAM	PRO-GRAM	PRO-GRAM	PRO-GRAM
U1	U1	I/O, PGCK4 (A1)	I/O, PGCK4 (A1)	I/O, PGCK4 (A1)	I/O, PGCK4 (A1)	I/O, PGCK4 (A1)
U2	U2	O, TDO	O, TDO	O, TDO	O, TDO	O, TDO
U3	U3	I/O (D0, DIN)	I/O (D0, DIN)	I/O (D0, DIN)	I/O (D0, DIN)	I/O (D0, DIN)
U4	U4	I/O	I/O	I/O	I/O	I/O
U5	U5	I/O	I/O	I/O	I/O	I/O
U6	U6	I/O	I/O	I/O	I/O	I/O
U7	U7	I/O	I/O	I/O	I/O	I/O
U8	U8	I/O	I/O	I/O	I/O	I/O
U9	U9	I/O (RS)	I/O (RS)	I/O (RS)	I/O (RS)	I/O (RS)
U10	U10	I/O (D4)	I/O (D4)	I/O (D4)	I/O (D4)	I/O (D4)
U11	U11	I/O	I/O	I/O	I/O	I/O
U12	U12	I/O (D5)	I/O (D5)	I/O (D5)	I/O (D5)	I/O (D5)
U13	U13	I/O	I/O	I/O	I/O	I/O
U14	U14	I/O	I/O	I/O	I/O	I/O
U15	U15	I/O	I/O	I/O	I/O	I/O
U16	U16	I/O, PGCK3	I/O, PGCK3	I/O, PGCK3	I/O, PGCK3	I/O, PGCK3
U17	U17	DONE	DONE	DONE	DONE	DONE
U18	U18	I/O	I/O	I/O	I/O	I/O
T1	T1	I/O	I/O	I/O	I/O	I/O
T2	T2	I/O (CS1,A2)	I/O (CS1,A2)	I/O (CS1,A2)	I/O (CS1,A2)	I/O (CS1,A2)
T3	T3	I/O (A0, WS)	I/O (A0, WS)	I/O (A0, WS)	I/O (A0, WS)	I/O (A0, WS)
T4	T4	I/O, SGCK4 (DOUT)	I/O, SGCK4 (DOUT)	I/O, SGCK4 (DOUT)	I/O, SGCK4 (DOUT)	I/O, SGCK4 (DOUT)
T5	T5	I/O	I/O	I/O	I/O	I/O
T6	T6	I/O	I/O	I/O	I/O	I/O
T7	T7	GND	GND	GND	GND	GND
T8	T8	I/O	I/O	I/O	I/O	I/O
T9	T9	I/O (D3)	I/O (D3)	I/O (D3)	I/O (D3)	I/O (D3)
T10	T10	I/O	I/O	I/O	I/O	I/O
T11	T11	I/O	I/O	I/O	I/O	I/O
T12	T12	GND	GND	GND	GND	GND
T13	T13	I/O	I/O	I/O	I/O	I/O
T14	T14	I/O	I/O	I/O	I/O	I/O
T15	T15	I/O (D7)	I/O (D7)	I/O (D7)	I/O (D7)	I/O (D7)
T16	T16	I/O, SGCK3	I/O, SGCK3	I/O, SGCK3	I/O, SGCK3	I/O, SGCK3
T17	T17	I/O	I/O	I/O	I/O	I/O
T18	T18	I/O	I/O	I/O	I/O	I/O
R1	R1	N.C.	I/O	I/O	I/O	I/O
R2	R2	I/O	I/O	I/O	I/O	I/O
R3	R3	GND	GND	GND	GND	GND
R4	R4	VCC	VCC	VCC	VCC	VCC
R5				I/O	I/O	I/O
R6				I/O	I/O	I/O
R7				I/O	I/O	I/O
R8				I/O	I/O	I/O
R9	R9	GND	GND	GND	GND	GND
R10	R10	VCC	VCC	VCC	VCC	VCC
R11				I/O	I/O	I/O
R12				I/O	I/O	I/O
R13				I/O	I/O	I/O
R14				I/O	I/O	I/O
R15	R15	VCC	VCC	VCC	VCC	VCC
R16	R16	GND	GND	GND	GND	GND
R17	R17	I/O	I/O	I/O	I/O	I/O
R18	R18	N.C.	I/O	I/O	I/O	I/O
P1	P1	I/O	I/O	I/O	I/O	I/O
P2	P2	I/O	I/O	I/O	I/O	I/O
P3	P3	I/O	I/O	I/O	I/O	I/O
P4				I/O	I/O	I/O
P15				I/O	I/O	I/O
P16	P16	I/O	I/O	I/O	I/O	I/O
P17	P17	I/O	I/O	I/O	I/O	I/O
P18	P18	I/O	I/O	I/O	I/O	I/O
N1	N1	I/O	I/O	I/O	I/O	I/O
N2	N2	N.C.	I/O	I/O	I/O	I/O
N3	N3	I/O (A3)	I/O (A3)	I/O (A3)	I/O (A3)	I/O (A3)
N4				I/O	I/O	I/O
N15				I/O	I/O	I/O
N16	N16	I/O	I/O	I/O	I/O	I/O

PG 223 Pin	PG 191 Pin	XC4008E PG191	XC4010E PG191	XC4013E PG223	XC4020E PG223	XC4025E PG223
N17	N17	N.C.	I/O	I/O	I/O	I/O
N18	N18	I/O	I/O	I/O	I/O	I/O
M1	M1	I/O (A5)	I/O (A5)	I/O (A5)	I/O (A5)	I/O (A5)
M2	M2	I/O (A4)	I/O (A4)	I/O (A4)	I/O (A4)	I/O (A4)
M3	M3	GND	GND	GND	GND	GND
M4				I/O	I/O	I/O
M15				I/O	I/O	I/O
M16	M16	GND	GND	GND	GND	GND
M17	M17	I/O	I/O	I/O	I/O	I/O
M18	M18	I/O	I/O	I/O	I/O	I/O
L1	L1	I/O	I/O	I/O	I/O	I/O
L2	L2	I/O	I/O	I/O	I/O	I/O
L3	L3	I/O	I/O	I/O	I/O	I/O
L4				I/O	I/O	I/O
L15				I/O	I/O	I/O
L16	L16	I/O	I/O	I/O	I/O	I/O
L17	L17	I/O	I/O	I/O	I/O	I/O
L18	L18	I/O	I/O	I/O	I/O	I/O
K1	K1	I/O	I/O	I/O	I/O	I/O
K2	K2	I/O (A6)	I/O (A6)	I/O (A6)	I/O (A6)	I/O (A6)
K3	K3	I/O (A7)	I/O (A7)	I/O (A7)	I/O (A7)	I/O (A7)
K4	K4	GND	GND	GND	GND	GND
K15	K15	GND	GND	GND	GND	GND
K16	K16	I/O	I/O	I/O	I/O	I/O
K17	K17	I/O	I/O	I/O	I/O	I/O
K18	K18	I/O	I/O	I/O	I/O	I/O
J1	J1	I/O	I/O	I/O	I/O	I/O
J2	J2	I/O (A9)	I/O (A9)	I/O (A9)	I/O (A9)	I/O (A9)
J3	J3	I/O (A8)	I/O (A8)	I/O (A8)	I/O (A8)	I/O (A8)
J4	J4	VCC	VCC	VCC	VCC	VCC
J15	J15	VCC	VCC	VCC	VCC	VCC
J16	J16	I/O ($\overline{\text{INIT}}$)	I/O ($\overline{\text{INIT}}$)	I/O ($\overline{\text{INIT}}$)	I/O ($\overline{\text{INIT}}$)	I/O ($\overline{\text{INIT}}$)
J17	J17	I/O	I/O	I/O	I/O	I/O
J18	J18	I/O	I/O	I/O	I/O	I/O
H1	H1	I/O	I/O	I/O	I/O	I/O
H2	H2	I/O	I/O	I/O	I/O	I/O
H3	H3	I/O	I/O	I/O	I/O	I/O
H4				I/O	I/O	I/O
H15				I/O	I/O	I/O
H16	H16	I/O	I/O	I/O	I/O	I/O
H17	H17	I/O	I/O	I/O	I/O	I/O
H18	H18	I/O	I/O	I/O	I/O	I/O
G1	G1	I/O (A10)	I/O (A10)	I/O (A10)	I/O (A10)	I/O (A10)
G2	G2	I/O (A11)	I/O (A11)	I/O (A11)	I/O (A11)	I/O (A11)
G3	G3	GND	GND	GND	GND	GND
G4				I/O	I/O	I/O
G15				I/O	I/O	I/O
G16	G16	GND	GND	GND	GND	GND
G17	G17	I/O	I/O	I/O	I/O	I/O
G18	G18	I/O	I/O	I/O	I/O	I/O
F1	F1	I/O	I/O	I/O	I/O	I/O

PG 223 Pin	PG 191 Pin	XC4008E PG191	XC4010E PG191	XC4013E PG223	XC4020E PG223	XC4025E PG223
F2	F2	N.C.	I/O	I/O	I/O	I/O
F3	F3	I/O (A12)	I/O (A12)	I/O (A12)	I/O (A12)	I/O (A12)
F4				I/O	I/O	I/O
F15				I/O	I/O	I/O
F16	F16	I/O	I/O	I/O	I/O	I/O
F17	F17	N.C.	I/O	I/O	I/O	I/O
F18	F18	I/O	I/O	I/O	I/O	I/O
E1	E1	I/O	I/O	I/O	I/O	I/O
E2	E2	I/O	I/O	I/O	I/O	I/O
E3	E3	I/O	I/O	I/O	I/O	I/O
E4				I/O	I/O	I/O
E15				I/O	I/O	I/O
E16	E16	I/O (HDC)	I/O (HDC)	I/O (HDC)	I/O (HDC)	I/O (HDC)
E17	E17	I/O ($\overline{\text{LDC}}$)	I/O ($\overline{\text{LDC}}$)	I/O ($\overline{\text{LDC}}$)	I/O ($\overline{\text{LDC}}$)	I/O ($\overline{\text{LDC}}$)
E18	E18	I/O	I/O	I/O	I/O	I/O
D1	D1	N.C.	I/O	I/O	I/O	I/O
D2	D2	I/O (A13)	I/O (A13)	I/O (A13)	I/O (A13)	I/O (A13)
D3	D3	VCC	VCC	VCC	VCC	VCC
D4	D4	GND	GND	GND	GND	GND
D5				I/O	I/O	I/O
D6				I/O	I/O	I/O
D7				I/O	I/O	I/O
D8				I/O	I/O	I/O
D9	D9	GND	GND	GND	GND	GND
D10	D10	VCC	VCC	VCC	VCC	VCC
D11				I/O	I/O	I/O
D12				I/O	I/O	I/O
D13				I/O	I/O	I/O
D14				I/O	I/O	I/O
D15	D15	GND	GND	GND	GND	GND
D16	D16	VCC	VCC	VCC	VCC	VCC
D17	D17	I/O	I/O	I/O	I/O	I/O
D18	D18	N.C.	I/O	I/O	I/O	I/O
C1	C1	I/O	I/O	I/O	I/O	I/O
C2	C2	I/O (A14)	I/O (A14)	I/O (A14)	I/O (A14)	I/O (A14)
C3	C3	I/O, PGCK1 (A16)	I/O, PGCK1 (A16)	I/O, PGCK1 (A16)	I/O, PGCK1 (A16)	I/O, PGCK1 (A16)
C4	C4	I/O (A17)	I/O (A17)	I/O (A17)	I/O (A17)	I/O (A17)
C5	C5	I/O	I/O	I/O	I/O	I/O
C6	C6	I/O	I/O	I/O	I/O	I/O
C7	C7	GND	GND	GND	GND	GND
C8	C8	I/O	I/O	I/O	I/O	I/O
C9	C9	I/O	I/O	I/O	I/O	I/O
C10	C10	I/O	I/O	I/O	I/O	I/O
C11	C11	I/O	I/O	I/O	I/O	I/O
C12	C12	GND	GND	GND	GND	GND
C13	C13	I/O	I/O	I/O	I/O	I/O
C14	C14	I/O	I/O	I/O	I/O	I/O
C15	C15	O (M1)	O (M1)	O (M1)	O (M1)	O (M1)
C16	C16	I (M2)	I (M2)	I (M2)	I (M2)	I (M2)

PG 223 Pin	PG 191 Pin	XC4008E PG191	XC4010E PG191	XC4013E PG223	XC4020E PG223	XC4025E PG223
C17	C17	I/O	I/O	I/O	I/O	I/O
C18	C18	I/O	I/O	I/O	I/O	I/O
B1	B1	I/O	I/O	I/O	I/O	I/O
B2	B2	I/O, SGCK1 (A15)	I/O, SGCK1 (A15)	I/O, SGCK1 (A15)	I/O, SGCK1 (A15)	I/O, SGCK1 (A15)
B3	B3	I/O	I/O	I/O	I/O	I/O
B4	B4	I/O, TCK	I/O, TCK	I/O, TCK	I/O, TCK	I/O, TCK
B5	**B5**	**N.C.**	**I/O**	I/O	I/O	I/O
B6	**B6**	**N.C.**	**I/O**	I/O	I/O	I/O
B7	B7	I/O, TMS	I/O, TMS	I/O, TMS	I/O, TMS	I/O, TMS
B8	B8	I/O	I/O	I/O	I/O	I/O
B9	B9	I/O	I/O	I/O	I/O	I/O
B10	B10	I/O	I/O	I/O	I/O	I/O
B11	B11	I/O	I/O	I/O	I/O	I/O
B12	B12	I/O	I/O	I/O	I/O	I/O
B13	**B13**	**N.C.**	**I/O**	I/O	I/O	I/O
B14	B14	I/O	I/O	I/O	I/O	I/O
B15	B15	I/O	I/O	I/O	I/O	I/O
B16	B16	I/O, SCGK2	I/O, SCGK2	I/O, SCGK2	I/O, SCGK2	I/O, SCGK2
B17	B17	I/O, PGCK2	I/O, PGCK2	I/O, PGCK2	I/O, PGCK2	I/O, PGCK2
B18	B18	I/O	I/O	I/O	I/O	I/O
A2	A2	I/O, TDI	I/O, TDI	I/O, TDI	I/O, TDI	I/O, TDI
A3	A3	I/O	I/O	I/O	I/O	I/O
A4	A4	I/O	I/O	I/O	I/O	I/O
A5	A5	I/O	I/O	I/O	I/O	I/O
A6	A6	I/O	I/O	I/O	I/O	I/O
A7	A7	I/O	I/O	I/O	I/O	I/O
A8	A8	I/O	I/O	I/O	I/O	I/O
A9	A9	I/O	I/O	I/O	I/O	I/O
A10	A10	I/O	I/O	I/O	I/O	I/O
A11	A11	I/O	I/O	I/O	I/O	I/O
A12	A12	I/O	I/O	I/O	I/O	I/O
A13	A13	I/O	I/O	I/O	I/O	I/O
A14	**A14**	**N.C.**	**I/O**	I/O	I/O	I/O
A15	A15	I/O	I/O	I/O	I/O	I/O
A16	A16	I/O	I/O	I/O	I/O	I/O
A17	A17	I/O	I/O	I/O	I/O	I/O
A18	A18	I (M0)	I (M0)	I (M0)	I (M0)	I (M0)

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Note: Shaded pins should be taken into account when designing PC boards, in case of future replacement by different devices.

Note: Viewed from the bottom side, the package pins start at the top row and go from the left edge to the right edge. Viewed from the top side, the pins start at the top row and go from the right edge to the left edge.

BG225 Package Pinouts

BG225 Pin	XC4010E	XC4013E/L
R1	VCC	VCC
R2	I/O, PGCK2	I/O, PGCK2
R3	I/O	I/O
R4	I/O	I/O
R5	I/O	I/O
R6	I/O	I/O
R7	I/O	I/O
R8	VCC	VCC
R9	I/O	I/O
R10	**N.C.**	**I/O**
R11	I/O	I/O
R12	I/O	I/O
R13	I/O	I/O
R14	I/O	I/O
R15	VCC	VCC
P1	I/O, SCGK2	I/O, SCGK2
P2	I (M0)	I (M0)
P3	I/O (HDC)	I/O (HDC)
P4	I/O ($\overline{LDC}$)	I/O ($\overline{LDC}$)
P5	**N.C.**	**I/O**
P6	I/O	I/O
P7	**N.C.**	**I/O**
P8	I/O ($\overline{INIT}$)	I/O ($\overline{INIT}$)
P9	I/O	I/O
P10	**N.C.**	**I/O**
P11	I/O	I/O
P12	I/O	I/O
P13	I/O	I/O
P14	DONE	DONE
P15	I/O (D7)	I/O (D7)
N1	I/O	I/O
N2	I/O	I/O
N3	O (M1)	O (M1)
N4	I/O	I/O
N5	I/O	I/O
N6	I/O	I/O
N7	**N.C.**	**I/O**
N8	I/O	I/O
N9	I/O	I/O
N10	I/O	I/O
N11	**N.C.**	**I/O**
N12	I/O	I/O
N13	I/O, SGCK3	I/O, SGCK3
N14	I/O, PGCK3	I/O, PGCK3
N15	**N.C.**	**I/O**
M1	I/O	I/O
M2	I/O	I/O
M3	I/O	I/O
M4	I (M2)	I (M2)
M5	I/O	I/O
M6	I/O	I/O
M7	I/O	I/O
M8	GND	GND
M9	I/O	I/O
M10	**N.C.**	**I/O**
M11	I/O	I/O
M12	$\overline{PROGRAM}$	$\overline{PROGRAM}$
M13	I/O	I/O

BG225 Pin	XC4010E	XC4013E/L
M14	**N.C.**	**I/O**
M15	I/O	I/O
L1	I/O	I/O
L2	**N.C.**	**I/O**
L3	I/O	I/O
L4	I/O	I/O
L5	I/O	I/O
L6	**N.C.**	**I/O**
L7	I/O	I/O
L8	I/O	I/O
L9	I/O	I/O
L10	I/O	I/O
L11	I/O	I/O
L12	I/O	I/O
L13	I/O	I/O
L14	I/O	I/O
L15	**N.C.**	**I/O**
K1	**N.C.**	**I/O**
K2	I/O	I/O
K3	I/O	I/O
K4	**N.C.**	**I/O**
K5	I/O	I/O
K6	I/O	I/O
K7	I/O	I/O
K8	GND	GND
K9	I/O	I/O
K10	I/O	I/O
K11	I/O	I/O
K12	**N.C.**	**I/O**
K13	I/O	I/O
K14	I/O	I/O
K15	I/O (D5)	I/O (D5)
J1	I/O	I/O
J2	I/O	I/O
J3	I/O	I/O
J4	I/O	I/O
J5	**N.C.**	**I/O**
J6	I/O	I/O
J7	GND	GND
J8	GND	GND
J9	GND	GND
J10	I/O (D6)	I/O (D6)
J11	I/O	I/O
J12	I/O ($\overline{CS0}$)	I/O ($\overline{CS0}$)
J13	I/O	I/O
J14	I/O	I/O
J15	I/O	I/O
H1	VCC	VCC
H2	GND	GND
H3	I/O	I/O
H4	I/O	I/O
H5	I/O	I/O
H6	GND	GND
H7	GND	GND
H8	GND	GND
H9	GND	GND
H10	GND	GND
H11	I/O ($\overline{RS}$)	I/O ($\overline{RS}$)
H12	I/O (D3)	I/O (D3)
H13	I/O (D4)	I/O (D4)

BG225 Pin	XC4010E	XC4013E/L
H14	I/O	I/O
H15	VCC	VCC
G1	I/O	I/O
G2	I/O	I/O
G3	I/O	I/O
G4	I/O	I/O
G5	I/O	I/O
G6	I/O	I/O
G7	GND	GND
G8	GND	GND
G9	GND	GND
G10	N.C.	I/O
G11	I/O (D2)	I/O (D2)
G12	I/O	I/O
G13	I/O	I/O
G14	I/O	I/O
G15	I/O	I/O
F1	N.C.	I/O
F2	N.C.	I/O
F3	I/O	I/O
F4	I/O, TMS	I/O, TMS
F5	I/O	I/O
F6	I/O	I/O
F7	N.C.	I/O
F8	GND	GND
F9	N.C.	I/O
F10	I/O (D0, DIN)	I/O (D0, DIN)
F11	I/O	I/O
F12	N.C.	I/O
F13	I/O	I/O
F14	I/O	I/O
F15	I/O	I/O
E1	I/O	I/O
E2	N.C.	I/O
E3	N.C.	I/O
E4	I/O	I/O
E5	I/O	I/O
E6	I/O	I/O
E7	I/O	I/O
E8	I/O (A8)	I/O (A8)
E9	I/O	I/O
E10	I/O	I/O
E11	I/O	I/O
E12	I/O (D1)	I/O (D1)
E13	I/O	I/O
E14	N.C.	I/O
E15	N.C.	I/O
D1	I/O	I/O
D2	I/O	I/O
D3	I/O, TDI	I/O, TDI
D4	I/O, PGCK1 (A16)	I/O, PGCK1 (A16)
D5	I/O (A13)	I/O (A13)
D6	I/O	I/O
D7	I/O	I/O
D8	VCC	VCC
D9	I/O (A5)	I/O (A5)
D10	I/O	I/O
D11	N.C.	I/O
D12	GND	GND
D13	I/O	I/O
D14	I/O	I/O
D15	I/O	I/O
C1	I/O, TCK	I/O, TCK
C2	I/O	I/O
C3	I/O, SGCK1 (A15)	I/O, SGCK1 (A15)
C4	N.C.	I/O
C5	I/O	I/O
C6	N.C.	I/O
C7	I/O	I/O
C8	I/O (A6)	I/O (A6)
C9	I/O	I/O
C10	N.C.	I/O
C11	I/O	I/O
C12	I/O	I/O
C13	CCLK	CCLK
C14	I/O	I/O
C15	I/O ($\overline{RCLK}$, RDY/$\overline{BUSY}$)	I/O ($\overline{RCLK}$, RDY/$\overline{BUSY}$)
B1	I/O (A17)	I/O (A17)
B2	VCC	VCC
B3	I/O	I/O
B4	I/O (A12)	I/O (A12)
B5	I/O	I/O
B6	I/O (A11)	I/O (A11)
B7	I/O (A9)	I/O (A9)
B8	I/O (A7)	I/O (A7)
B9	I/O	I/O
B10	N.C.	I/O
B11	I/O	I/O
B12	I/O (A3)	I/O (A3)
B13	I/O, PGCK4 (A1)	I/O, PGCK4 (A1)
B14	VCC	VCC
B15	I/O, SGCK4 (DOUT)	I/O, SGCK4 (DOUT)
A1	GND	GND
A2	I/O (A14)	I/O (A14)
A3	N.C.	I/O
A4	I/O	I/O
A5	I/O	I/O
A6	I/O (A10)	I/O (A10)
A7	I/O	I/O
A8	GND	GND
A9	I/O	I/O
A10	I/O (A4)	I/O (A4)
A11	I/O	I/O
A12	I/O	I/O
A13	I/O (CS1, A2)	I/O (CS1, A2)
A14	I/O (A0, $\overline{WS}$)	I/O (A0, $\overline{WS}$)
A15	O, TDO	O, TDO

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PQ240, HQ240 Package Pinouts

PQ240/ HQ240 Pin	XC4013E XC4013L	XC4020E	XC4025E	XC4028EX XC4028XL
P1	GND	GND	GND	GND
P2	I/O, PGCK1 (A16)	I/O, PGCK1 (A16)	I/O, PGCK1 (A16)	I/O, GCK1 (A16)
P3	I/O (A17)	I/O (A17)	I/O (A17)	I/O (A17)
P4	I/O	I/O	I/O	I/O
P5	I/O	I/O	I/O	I/O
P6	I/O, TDI	I/O, TDI	I/O, TDI	I/O, TDI
P7	I/O, TCK	I/O, TCK	I/O, TCK	I/O, TCK
P8	I/O	I/O	I/O	I/O
P9	I/O	I/O	I/O	I/O
P10	I/O	I/O	I/O	I/O
P11	I/O	I/O	I/O	I/O
P12	I/O	I/O	I/O	I/O
P13	I/O	I/O	I/O	I/O
P14	GND	GND	GND	GND
P15	I/O	I/O	I/O	I/O, FCLK1
P16	I/O	I/O	I/O	I/O
P17	I/O, TMS	I/O, TMS	I/O, TMS	I/O, TMS
P18	I/O	I/O	I/O	I/O
P19	VCC	VCC	VCC	VCC
P20	I/O	I/O	I/O	I/O
P21	I/O	I/O	I/O	I/O
P22	**N.C.‡**	**N.C.‡**	**N.C.‡**	**GND‡**
P23	I/O	I/O	I/O	I/O
P24	I/O	I/O	I/O	I/O
P25	I/O	I/O	I/O	I/O
P26	I/O	I/O	I/O	I/O
P27	I/O	I/O	I/O	I/O
P28	I/O	I/O	I/O	I/O
P29	GND	GND	GND	GND
P30	VCC	VCC	VCC	VCC
P31	I/O	I/O	I/O	I/O
P32	I/O	I/O	I/O	I/O
P33	I/O	I/O	I/O	I/O
P34	I/O	I/O	I/O	I/O
P35	I/O	I/O	I/O	I/O
P36	I/O	I/O	I/O	I/O
P37	**N.C.‡**	**N.C.‡**	**N.C.‡**	**GND‡**
P38	I/O	I/O	I/O	I/O
P39	I/O	I/O	I/O	I/O
P40	VCC	VCC	VCC	VCC
P41	I/O	I/O	I/O	I/O
P42	I/O	I/O	I/O	I/O
P43	I/O	I/O	I/O	I/O
P44	I/O	I/O	I/O	I/O, FCLK2
P45	GND	GND	GND	GND
P46	I/O	I/O	I/O	I/O
P47	I/O	I/O	I/O	I/O
P48	I/O	I/O	I/O	I/O
P49	I/O	I/O	I/O	I/O
P50	I/O	I/O	I/O	I/O
P51	I/O	I/O	I/O	I/O
P52	I/O	I/O	I/O	I/O
P53	I/O	I/O	I/O	I/O
P54	I/O	I/O	I/O	I/O
P55	I/O	I/O	I/O	I/O
P56	I/O	I/O	I/O	I/O
P57	I/O, SGCK2	I/O, SGCK2	I/O, SGCK2	I/O, GCK2
P58	O (M1)	O (M1)	O (M1)	O (M1)
P59	GND	GND	GND	GND
P60	I (M0)	I (M0)	I (M0)	I (M0)
P61	VCC	VCC	VCC	VCC
P62	I (M2)	I (M2)	I (M2)	I (M2)
P63	I/O, PGCK2	I/O, PGCK2	I/O, PGCK2	I/O, GCK3
P64	I/O (HDC)	I/O (HDC)	I/O (HDC)	I/O (HDC)
P65	I/O	I/O	I/O	I/O
P66	I/O	I/O	I/O	I/O
P67	I/O	I/O	I/O	I/O
P68	I/O ($\overline{\text{LDC}}$)	I/O ($\overline{\text{LDC}}$)	I/O ($\overline{\text{LDC}}$)	I/O ($\overline{\text{LDC}}$)
P69	I/O	I/O	I/O	I/O
P70	I/O	I/O	I/O	I/O
P71	I/O	I/O	I/O	I/O
P72	I/O	I/O	I/O	I/O
P73	I/O	I/O	I/O	I/O
P74	I/O	I/O	I/O	I/O
P75	GND	GND	GND	GND
P76	I/O	I/O	I/O	I/O
P77	I/O	I/O	I/O	I/O
P78	I/O	I/O	I/O	I/O
P79	I/O	I/O	I/O	I/O
P80	VCC	VCC	VCC	VCC
P81	I/O	I/O	I/O	I/O
P82	I/O	I/O	I/O	I/O
P83	**N.C.‡**	**N.C.‡**	**N.C.‡**	**GND‡**
P84	I/O	I/O	I/O	I/O
P85	I/O	I/O	I/O	I/O
P86	I/O	I/O	I/O	I/O
P87	I/O	I/O	I/O	I/O
P88	I/O	I/O	I/O	I/O
P89	I/O ($\overline{\text{INIT}}$)	I/O ($\overline{\text{INIT}}$)	I/O ($\overline{\text{INIT}}$)	I/O ($\overline{\text{INIT}}$)

PQ240/ HQ240 Pin	XC4013E XC4013L	XC4020E	XC4025E	XC4028EX XC4028XL
P90	VCC	VCC	VCC	VCC
P91	GND	GND	GND	GND
P92	I/O	I/O	I/O	I/O
P93	I/O	I/O	I/O	I/O
P94	I/O	I/O	I/O	I/O
P95	I/O	I/O	I/O	I/O
P96	I/O	I/O	I/O	I/O
P97	I/O	I/O	I/O	I/O
P98	**N.C.‡**	**N.C.‡**	**N.C.‡**	**GND‡**
P99	I/O	I/O	I/O	I/O
P100	I/O	I/O	I/O	I/O
P101	VCC	VCC	VCC	VCC
P102	I/O	I/O	I/O	I/O
P103	I/O	I/O	I/O	I/O
P104	I/O	I/O	I/O	I/O
P105	I/O	I/O	I/O	I/O
P106	GND	GND	GND	GND
P107	I/O	I/O	I/O	I/O
P108	I/O	I/O	I/O	I/O
P109	I/O	I/O	I/O	I/O
P110	I/O	I/O	I/O	I/O
P111	I/O	I/O	I/O	I/O
P112	I/O	I/O	I/O	I/O
P113	I/O	I/O	I/O	I/O
P114	I/O	I/O	I/O	I/O
P115	I/O	I/O	I/O	I/O
P116	I/O	I/O	I/O	I/O
P117	I/O	I/O	I/O	I/O
P118	I/O, SGCK3	I/O, SGCK3	I/O, SGCK3	I/O, GCK4
P119	GND	GND	GND	GND
P120	DONE	DONE	DONE	DONE
P121	VCC	VCC	VCC	VCC
P122	$\overline{\text{PROGRAM}}$	$\overline{\text{PROGRAM}}$	$\overline{\text{PROGRAM}}$	$\overline{\text{PROGRAM}}$
P123	I/O (D7)	I/O (D7)	I/O (D7)	I/O (D7)
P124	I/O, PGCK3	I/O, PGCK3	I/O, PGCK3	I/O, GCK5
P125	I/O	I/O	I/O	I/O
P126	I/O	I/O	I/O	I/O
P127	I/O	I/O	I/O	I/O
P128	I/O	I/O	I/O	I/O
P129	I/O (D6)	I/O (D6)	I/O (D6)	I/O (D6)
P130	I/O	I/O	I/O	I/O
P131	I/O	I/O	I/O	I/O
P132	I/O	I/O	I/O	I/O
P133	I/O	I/O	I/O	I/O

PQ240/ HQ240 Pin	XC4013E XC4013L	XC4020E	XC4025E	XC4028EX XC4028XL
P134	I/O	I/O	I/O	I/O
P135	GND	GND	GND	GND
P136	I/O	I/O	I/O	I/O
P137	I/O	I/O	I/O	I/O
P138	I/O	I/O	I/O	I/O, FCLK3
P139	I/O	I/O	I/O	I/O
P140	VCC	VCC	VCC	VCC
P141	I/O (D5)	I/O (D5)	I/O (D5)	I/O (D5)
P142	I/O ($\overline{\text{CS0}}$)	I/O ($\overline{\text{CS0}}$)	I/O ($\overline{\text{CS0}}$)	I/O ($\overline{\text{CS0}}$)
P143	**N.C.‡**	**N.C.‡**	**N.C.‡**	**GND‡**
P144	I/O	I/O	I/O	I/O
P145	I/O	I/O	I/O	I/O
P146	I/O	I/O	I/O	I/O
P147	I/O	I/O	I/O	I/O
P148	I/O (D4)	I/O (D4)	I/O (D4)	I/O (D4)
P149	I/O	I/O	I/O	I/O
P150	VCC	VCC	VCC	VCC
P151	GND	GND	GND	GND
P152	I/O (D3)	I/O (D3)	I/O (D3)	I/O (D3)
P153	I/O ($\overline{\text{RS}}$)	I/O ($\overline{\text{RS}}$)	I/O ($\overline{\text{RS}}$)	I/O ($\overline{\text{RS}}$)
P154	I/O	I/O	I/O	I/O
P155	I/O	I/O	I/O	I/O
P156	I/O	I/O	I/O	I/O
P157	I/O	I/O	I/O	I/O
P158	**N.C.‡**	**N.C.‡**	**N.C.‡**	**GND‡**
P159	I/O (D2)	I/O (D2)	I/O (D2)	I/O (D2)
P160	I/O	I/O	I/O	I/O
P161	VCC	VCC	VCC	VCC
P162	I/O	I/O	I/O	I/O
P163	I/O	I/O	I/O	I/O, FCLK4
P164	I/O	I/O	I/O	I/O
P165	I/O	I/O	I/O	I/O
P166	GND	GND	GND	GND
P167	I/O	I/O	I/O	I/O
P168	I/O	I/O	I/O	I/O
P169	I/O	I/O	I/O	I/O
P170	I/O	I/O	I/O	I/O
P171	I/O	I/O	I/O	I/O
P172	I/O	I/O	I/O	I/O
P173	I/O (D1)	I/O (D1)	I/O (D1)	I/O (D1)
P174	I/O ($\overline{\text{RCLK}}$, RDY/ $\overline{\text{BUSY}}$)	I/O ($\overline{\text{RCLK}}$, RDY/ $\overline{\text{BUSY}}$)	I/O ($\overline{\text{RCLK}}$, RDY/ $\overline{\text{BUSY}}$)	I/O ($\overline{\text{RCLK}}$, RDY/ $\overline{\text{BUSY}}$)
P175	I/O	I/O	I/O	I/O
P176	I/O	I/O	I/O	I/O

PQ240/ HQ240 Pin	XC4013E XC4013L	XC4020E	XC4025E	XC4028EX XC4028XL
P177	I/O (D0, DIN)	I/O (D0, DIN)	I/O (D0, DIN)	I/O (D0, DIN)
P178	I/O, SGCK4 (DOUT)	I/O, SGCK4 (DOUT)	I/O, SGCK4 (DOUT)	I/O, GCK6 (DOUT)
P179	CCLK	CCLK	CCLK	CCLK
P180	VCC	VCC	VCC	VCC
P181	O, TDO	O, TDO	O, TDO	O, TDO
P182	GND	GND	GND	GND
P183	I/O (A0, $\overline{WS}$)	I/O (A0, $\overline{WS}$)	I/O (A0, $\overline{WS}$)	I/O (A0, $\overline{WS}$)
P184	I/O, PGCK4 (A1)	I/O, PGCK4 (A1)	I/O, PGCK4 (A1)	I/O, GCK7 (A1)
P185	I/O	I/O	I/O	I/O
P186	I/O	I/O	I/O	I/O
P187	I/O (CS1, A2)	I/O (CS1, A2)	I/O (CS1, A2)	I/O (CS1, A2)
P188	I/O (A3)	I/O (A3)	I/O (A3)	I/O (A3)
P189	I/O	I/O	I/O	I/O
P190	I/O	I/O	I/O	I/O
P191	I/O	I/O	I/O	I/O
P192	I/O	I/O	I/O	I/O
P193	I/O	I/O	I/O	I/O
P194	I/O	I/O	I/O	I/O
P195	**N.C.**	**N.C.**	**I/O**	**I/O**
P196	GND	GND	GND	GND
P197	I/O	I/O	I/O	I/O
P198	I/O	I/O	I/O	I/O
P199	I/O	I/O	I/O	I/O
P200	I/O	I/O	I/O	I/O
P201	VCC	VCC	VCC	VCC
P202	I/O (A4)	I/O (A4)	I/O (A4)	I/O (A4)
P203	I/O (A5)	I/O (A5)	I/O (A5)	I/O (A5)
P204	**N.C.‡**	**N.C.‡**	**N.C.‡**	**GND‡**
P205	I/O	I/O	I/O	I/O
P206	I/O	I/O	I/O	I/O
P207	**I/O**	**I/O**	**I/O**	**I/O (A21)**
P208	**I/O**	**I/O**	**I/O**	**I/O (A20)**
P209	I/O (A6)	I/O (A6)	I/O (A6)	I/O (A6)
P210	I/O (A7)	I/O (A7)	I/O (A7)	I/O (A7)
P211	GND	GND	GND	GND
P212	VCC	VCC	VCC	VCC
P213	I/O (A8)	I/O (A8)	I/O (A8)	I/O (A8)
P214	I/O (A9)	I/O (A9)	I/O (A9)	I/O (A9)
P215	**I/O**	**I/O**	**I/O**	**I/O (A19)**
P216	**I/O**	**I/O**	**I/O**	**I/O (A18)**
P217	I/O	I/O	I/O	I/O
P218	I/O	I/O	I/O	I/O
P219	**N.C.‡**	**N.C.‡**	**N.C.‡**	**GND‡**
P220	I/O (A10)	I/O (A10)	I/O (A10)	I/O (A10)
P221	I/O (A11)	I/O (A11)	I/O (A11)	I/O (A11)
P222	VCC	VCC	VCC	VCC
P223	I/O	I/O	I/O	I/O
P224	I/O	I/O	I/O	I/O
P225	I/O	I/O	I/O	I/O
P226	I/O	I/O	I/O	I/O
P227	GND	GND	GND	GND
P228	I/O	I/O	I/O	I/O
P229	I/O	I/O	I/O	I/O
P230	I/O	I/O	I/O	I/O
P231	I/O	I/O	I/O	I/O
P232	I/O (A12)	I/O (A12)	I/O (A12)	I/O (A12)
P233	I/O (A13)	I/O (A13)	I/O (A13)	I/O (A13)
P234	I/O	I/O	I/O	I/O
P235	I/O	I/O	I/O	I/O
P236	I/O	I/O	I/O	I/O
P237	I/O	I/O	I/O	I/O
P238	I/O (A14)	I/O (A14)	I/O (A14)	I/O (A14)
P239	I/O, SGCK1 (A15)	I/O, SGCK1 (A15)	I/O, SGCK1 (A15)	I/O, GCK8 (A15)
P240	VCC	VCC	VCC	VCC

3/11/96

‡ Pins labelled GND‡ should be connected to Ground if possible; however, they can be left unconnected if necessary for compatibility with other devices. Pins labelled N.C.‡ *are reserved for Ground connections on future revisions of the device.* These pins do not physically connect to anything on the current device revision. However, they should be externally connected to Ground if possible.

Note: Shaded pins should be taken into account when designing PC boards, in case of future replacement by different devices.

PG299 Package Pinouts

PG299 Pin	XC4025E	XC4028EX/XL
X1	I/O, SGCK4 (DOUT)	I/O, GCK6 (DOUT)
X2	GND	GND
X3	I/O	I/O
X4	I/O	I/O
X5	VCC	VCC
X6	GND	GND
X7	I/O	I/O
X8	I/O	I/O
X9	I/O	I/O
X10	VCC	VCC
X11	GND	GND
X12	I/O	I/O
X13	I/O	I/O
X14	I/O ($\overline{CS0}$)	I/O ($\overline{CS0}$)
X15	VCC	VCC
X16	GND	GND
X17	I/O	I/O
X18	I/O	I/O
X19	VCC	VCC
X20	I/O, SGCK3	I/O, GCK4
W1	VCC	VCC
W2	I/O (A0, $\overline{WS}$)	I/O (A0, $\overline{WS}$)
W3	I/O	I/O
W4	I/O	I/O
W5	I/O	I/O
W6	I/O	I/O
W7	I/O	I/O, FCLK4
W8	I/O (D2)	I/O (D2)
W9	I/O	I/O
W10	I/O (D3)	I/O (D3)
W11	I/O	I/O
W12	I/O	I/O
W13	I/O	I/O
W14	I/O	I/O, FCLK3
W15	I/O	I/O
W16	I/O	I/O
W17	I/O (D6)	I/O (D6)
W18	I/O, PGCK3	I/O, GCK5
W19	I/O (D7)	I/O (D7)
W20	GND	GND
V1	I/O (A3)	I/O (A3)
V2	I/O, PGCK4 (A1)	I/O, GCK7 (A1)
V3	CCLK	CCLK
V4	I/O (D0, DIN)	I/O (D0, DIN)
V5	I/O ($\overline{RCLK}$, RDY/$\overline{BUSY}$)	I/O ($\overline{RCLK}$, RDY/$\overline{BUSY}$)
V6	I/O	I/O
V7	I/O	I/O
V8	I/O	I/O
V9	I/O	I/O
V10	I/O ($\overline{RS}$)	I/O ($\overline{RS}$)
V11	I/O (D4)	I/O (D4)
V12	I/O	I/O
V13	I/O	I/O
V14	I/O	I/O
V15	I/O	I/O
V16	I/O	I/O
V17	I/O	I/O
V18	DONE	DONE
V19	I/O	I/O
V20	I/O	I/O
U1	I/O	I/O
U2	I/O	I/O
U3	I/O (CS1, A2)	I/O (CS1, A2)
U4	O, TDO	O, TDO
U5	I/O	I/O
U6	I/O (D1)	I/O (D1)
U7	I/O	I/O
U8	I/O	I/O
U9	I/O	I/O
U10	I/O	I/O
U11	I/O	I/O
U12	I/O	I/O
U13	I/O	I/O
U14	I/O	I/O
U15	I/O	I/O
U16	I/O	I/O
U17	$\overline{PROGRAM}$	$\overline{PROGRAM}$
U18	I/O	I/O
U19	I/O	I/O
U20	I/O	I/O
T1	GND	GND
T2	I/O	I/O
T3	I/O	I/O
T4	I/O	I/O
T5	GND	GND
T6	I/O	I/O
T7	I/O	I/O
T8	I/O	I/O
T9	I/O	I/O
T10	I/O	I/O
T11	I/O	I/O
T12	I/O (D5)	I/O (D5)
T13	I/O	I/O
T14	I/O	I/O
T15	I/O	I/O
T16	VCC	VCC
T17	I/O	I/O
T18	I/O	I/O
T19	I/O	I/O
T20	VCC	VCC
R1	VCC	VCC
R2	I/O	I/O

PG299 Pin	XC4025E	XC4028EX/XL
R3	I/O	I/O
R4	I/O	I/O
R5	I/O	I/O
R16	I/O	I/O
R17	I/O	I/O
R18	I/O	I/O
R19	I/O	I/O
R20	GND	GND
P1	I/O	I/O
P2	I/O	I/O
P3	I/O	I/O
P4	I/O	I/O
P5	I/O	I/O
P16	I/O	I/O
P17	I/O	I/O
P18	I/O	I/O
P19	I/O	I/O
P20	I/O	I/O
N1	I/O (A4)	I/O (A4)
N2	I/O	I/O
N3	I/O	I/O
N4	I/O	I/O
N5	I/O	I/O
N16	I/O	I/O
N17	I/O	I/O
N18	I/O	I/O
N19	I/O	I/O
N20	I/O	I/O
M1	I/O	I/O (A21)
M2	I/O	I/O
M3	I/O (A5)	I/O (A5)
M4	I/O	I/O
M5	I/O	I/O
M16	I/O	I/O
M17	I/O	I/O
M18	I/O	I/O
M19	I/O	I/O
M20	I/O	I/O
L1	GND	GND
L2	I/O (A7)	I/O (A7)
L3	I/O (A6)	I/O (A6)
L4	I/O	I/O (A20)
L5	I/O	I/O
L16	I/O	I/O
L17	I/O	I/O
L18	I/O	I/O
L19	I/O	I/O
L20	VCC	VCC
K1	VCC	VCC
K2	I/O (A8)	I/O (A8)
K3	I/O (A9)	I/O (A9)
K4	I/O	I/O (A18)

PG299 Pin	XC4025E	XC4028EX/XL
K5	I/O	I/O (A19)
K16	I/O	I/O
K17	I/O	I/O
K18	I/O	I/O
K19	I/O ($\overline{\text{INIT}}$)	I/O ($\overline{\text{INIT}}$)
K20	GND	GND
J1	I/O	I/O
J2	I/O	I/O
J3	I/O (A11)	I/O (A11)
J4	I/O	I/O
J5	I/O	I/O
J16	I/O	I/O
J17	I/O	I/O
J18	I/O	I/O
J19	I/O	I/O
J20	I/O	I/O
H1	I/O (A10)	I/O (A10)
H2	I/O	I/O
H3	I/O	I/O
H4	I/O	I/O
H5	I/O	I/O
H16	I/O	I/O
H17	I/O	I/O
H18	I/O	I/O
H19	I/O	I/O
H20	I/O	I/O
G1	I/O	I/O
G2	I/O	I/O
G3	I/O	I/O
G4	I/O	I/O
G5	I/O (A12)	I/O (A12)
G16	I/O	I/O
G17	I/O	I/O
G18	I/O	I/O
G19	I/O	I/O
G20	I/O	I/O
F1	GND	GND
F2	I/O	I/O
F3	I/O	I/O
F4	I/O	I/O
F5	I/O	I/O
F16	I/O	I/O
F17	I/O	I/O
F18	I/O	I/O
F19	I/O	I/O
F20	VCC	VCC
E1	VCC	VCC
E2	I/O	I/O
E3	I/O	I/O
E4	I/O	I/O
E5	VCC	VCC
E6	I/O	I/O

PG299 Pin	XC4025E	XC4028EX/XL
E7	I/O	I/O
E8	I/O	I/O
E9	I/O	I/O
E10	I/O	I/O
E11	I/O	I/O
E12	I/O	I/O
E13	I/O	I/O
E14	I/O	I/O
E15	I/O	I/O
E16	GND	GND
E17	I/O	I/O
E18	I/O	I/O
E19	I/O	I/O
E20	GND	GND
D1	I/O	I/O
D2	I/O	I/O
D3	I/O (A14)	I/O (A14)
D4	I/O, PGCK1 (A16)	I/O, GCK1 (A16)
D5	I/O, TDI	I/O, TDI
D6	I/O	I/O
D7	I/O	I/O
D8	I/O	I/O
D9	I/O	I/O
D10	I/O	I/O
D11	I/O	I/O
D12	I/O	I/O
D13	I/O	I/O, FCLK2
D14	I/O	I/O
D15	I/O	I/O
D16	I/O	I/O
D17	I (M2)	I (M2)
D18	I/O	I/O
D19	I/O	I/O
D20	I/O	I/O
C1	I/O (A13)	I/O (A13)
C2	I/O	I/O
C3	I/O, SGCK1 (A15)	I/O, GCK8 (A15)
C4	I/O, TCK	I/O, TCK
C5	I/O	I/O
C6	I/O	I/O
C7	I/O, TMS	I/O, TMS
C8	I/O	I/O
C9	I/O	I/O
C10	I/O	I/O
C11	I/O	I/O
C12	I/O	I/O
C13	I/O	I/O
C14	I/O	I/O
C15	I/O	I/O
C16	I/O	I/O
C17	I/O, SGCK2	I/O, GCK2
C18	I (M0)	I (M0)

PG299 Pin	XC4025E	XC4028EX/XL
C19	I/O (HDC)	I/O (HDC)
C20	I/O ($\overline{LDC}$)	I/O ($\overline{LDC}$)
B1	GND	GND
B2	I/O (A17)	I/O (A17)
B3	I/O	I/O
B4	I/O	I/O
B5	I/O	I/O
B6	I/O	I/O, FCLK1
B7	I/O	I/O
B8	I/O	I/O
B9	I/O	I/O
B10	I/O	I/O
B11	I/O	I/O
B12	I/O	I/O
B13	I/O	I/O
B14	I/O	I/O
B15	I/O	I/O
B16	I/O	I/O
B17	I/O	I/O
B18	I/O	I/O
B19	I/O, PGCK2	I/O, GCK3
B20	VCC	VCC
A2	VCC	VCC
A3	I/O	I/O
A4	I/O	I/O
A5	GND	GND
A6	VCC	VCC
A7	I/O	I/O
A8	I/O	I/O
A9	I/O	I/O
A10	GND	GND
A11	VCC	VCC
A12	I/O	I/O
A13	I/O	I/O
A14	I/O	I/O
A15	GND	GND
A16	VCC	VCC
A17	I/O	I/O
A18	I/O	I/O
A19	GND	GND
A20	O (M1)	O (M1)

3/18/96

Note: Shaded pins should be taken into account when designing PC boards, in case of future replacement by different devices.

Note: Viewed from the bottom side, the package pins start at the top row and go from the left edge to the right edge. Viewed from the top side, the pins start at the top row and go from the right edge to the left edge.

HQ304 Package Pinouts

HQ304 Pin	XC4025E	XC4028EX XC4028XL	XC4036EX XC4036XL
P1	VCC	VCC	VCC
P2	I/O, SGCK1 (A15)	I/O, GCK8 (A15)	I/O, GCK8 (A15)
P3	I/O (A14)	I/O (A14)	I/O (A14)
P4	I/O	I/O	I/O
P5	I/O	I/O	I/O
P6	I/O	I/O	I/O
P7	I/O	I/O	I/O
P8	I/O	I/O	I/O
P9	I/O	I/O	I/O
P10	I/O (A13)	I/O (A13)	I/O (A13)
P11	N.C.	N.C.	N.C.
P12	I/O (A12)	I/O (A12)	I/O (A12)
P13	I/O	I/O	I/O
P14	I/O	I/O	I/O
P15	I/O	I/O	I/O
P16	I/O	I/O	I/O
P17	I/O	I/O	I/O
P18	I/O	I/O	I/O
P19	GND	GND	GND
P20	I/O	I/O	I/O
P21	I/O	I/O	I/O
P22	I/O	I/O	I/O
P23	I/O	I/O	I/O
P24	N.C.	N.C.	N.C.
P25	VCC	VCC	VCC
P26	I/O	I/O	I/O
P27	I/O	I/O	I/O
P28	I/O	I/O	I/O
P29	I/O	I/O	I/O
P30	I/O (A11)	I/O (A11)	I/O (A11)
P31	I/O (A10)	I/O (A10)	I/O (A10)
P32	I/O	I/O	I/O
P33	I/O	I/O	I/O
P34	**I/O**	**I/O (A18)**	**I/O (A18)**
P35	**I/O**	**I/O (A19)**	**I/O (A19)**
P36	I/O (A9)	I/O (A9)	I/O (A9)
P37	I/O (A8)	I/O (A8)	I/O (A8)
P38	VCC	VCC	VCC
P39	GND	GND	GND
P40	I/O (A7)	I/O (A7)	I/O (A7)
P41	I/O (A6)	I/O (A6)	I/O (A6)
P42	**I/O**	**I/O (A20)**	**I/O (A20)**
P43	**I/O**	**I/O (A21)**	**I/O (A21)**
P44	I/O	I/O	I/O
P45	I/O	I/O	I/O
P46	I/O (A5)	I/O (A5)	I/O (A5)
P47	I/O (A4)	I/O (A4)	I/O (A4)
P48	I/O	I/O	I/O
P49	I/O	I/O	I/O
P50	I/O	I/O	I/O
P51	I/O	I/O	I/O
P52	VCC	VCC	VCC
P53	N.C.	N.C.	N.C.
P54	I/O	I/O	I/O
P55	I/O	I/O	I/O
P56	I/O	I/O	I/O
P57	I/O	I/O	I/O
P58	GND	GND	GND
P59	I/O	I/O	I/O
P60	I/O	I/O	I/O
P61	I/O	I/O	I/O
P62	I/O	I/O	I/O
P63	I/O	I/O	I/O
P64	I/O	I/O	I/O
P65	I/O	I/O	I/O
P66	I/O	I/O	I/O
P67	I/O	I/O	I/O
P68	I/O	I/O	I/O
P69	I/O (A3)	I/O (A3)	I/O (A3)
P70	I/O (CS1, A2)	I/O (CS1, A2)	I/O (CS1, A2)
P71	I/O	I/O	I/O
P72	I/O	I/O	I/O
P73	I/O, PGCK4 (A1)	I/O, GCK7 (A1)	I/O, GCK7 (A1)
P74	I/O (A0, $\overline{WS}$)	I/O (A0, $\overline{WS}$)	I/O (A0, $\overline{WS}$)
P75	GND	GND	GND
P76	O, TDO	O, TDO	O, TDO
P77	VCC	VCC	VCC
P78	CCLK	CCLK	CCLK
P79	I/O, SGCK4 (DOUT)	I/O, GCK6 (DOUT)	I/O, GCK6 (DOUT)
P80	I/O (D0, DIN)	I/O (D0, DIN)	I/O (D0, DIN)
P81	I/O	I/O	I/O
P82	I/O	I/O	I/O
P83	I/O	I/O	I/O
P84	I/O	I/O	I/O
P85	I/O ($\overline{RCLK}$, RDY/$\overline{BUSY}$)	I/O ($\overline{RCLK}$, RDY/$\overline{BUSY}$)	I/O ($\overline{RCLK}$, RDY/$\overline{BUSY}$)
P86	I/O (D1)	I/O (D1)	I/O (D1)
P87	I/O	I/O	I/O
P88	I/O	I/O	I/O
P89	I/O	I/O	I/O
P90	I/O	I/O	I/O
P91	I/O	I/O	I/O
P92	I/O	I/O	I/O
P93	I/O	I/O	I/O
P94	I/O	I/O	I/O
P95	GND	GND	GND
P96	I/O	I/O	I/O
P97	I/O	I/O	I/O
P98	I/O	I/O, FCLK4	I/O, FCLK4
P99	I/O	I/O	I/O
P100	N.C.	N.C.	N.C.
P101	VCC	VCC	VCC

HQ304 Pin	XC4025E	XC4028EX XC4028XL	XC4036EX XC4036XL
P102	I/O	I/O	I/O
P103	I/O (D2)	I/O (D2)	I/O (D2)
P104	I/O	I/O	I/O
P105	I/O	I/O	I/O
P106	I/O	I/O	I/O
P107	I/O	I/O	I/O
P108	I/O	I/O	I/O
P109	I/O	I/O	I/O
P110	I/O	I/O	I/O
P111	I/O	I/O	I/O
P112	I/O ($\overline{RS}$)	I/O ($\overline{RS}$)	I/O ($\overline{RS}$)
P113	I/O (D3)	I/O (D3)	I/O (D3)
P114	GND	GND	GND
P115	VCC	VCC	VCC
P116	I/O	I/O	I/O
P117	I/O (D4)	I/O (D4)	I/O (D4)
P118	I/O	I/O	I/O
P119	I/O	I/O	I/O
P120	I/O	I/O	I/O
P121	I/O	I/O	I/O
P122	I/O	I/O	I/O
P123	I/O	I/O	I/O
P124	I/O	I/O	I/O
P125	I/O	I/O	I/O
P126	I/O ($\overline{CS0}$)	I/O ($\overline{CS0}$)	I/O ($\overline{CS0}$)
P127	I/O (D5)	I/O (D5)	I/O (D5)
P128	N.C.	N.C.	N.C.
P129	VCC	VCC	VCC
P130	I/O	I/O	I/O
P131	I/O	I/O, FCLK3	I/O, FCLK3
P132	I/O	I/O	I/O
P133	I/O	I/O	I/O
P134	GND	GND	GND
P135	I/O	I/O	I/O
P136	I/O	I/O	I/O
P137	I/O	I/O	I/O
P138	I/O	I/O	I/O
P139	I/O	I/O	I/O
P140	I/O	I/O	I/O
P141	I/O	I/O	I/O
P142	I/O (D6)	I/O (D6)	I/O (D6)
P143	I/O	I/O	I/O
P144	I/O	I/O	I/O
P145	I/O	I/O	I/O
P146	I/O	I/O	I/O
P147	I/O	I/O	I/O
P148	I/O	I/O	I/O
P149	I/O, PGCK3	I/O, GCK5	I/O, GCK5
P150	I/O (D7)	I/O (D7)	I/O (D7)
P151	$\overline{PROGRAM}$	$\overline{PROGRAM}$	$\overline{PROGRAM}$
P152	VCC	VCC	VCC
P153	DONE	DONE	DONE
P154	GND	GND	GND

HQ304 Pin	XC4025E	XC4028EX XC4028XL	XC4036EX XC4036XL
P155	I/O, SGCK3	I/O, GCK4	I/O. GCK4
P156	I/O	I/O	I/O
P157	I/O	I/O	I/O
P158	I/O	I/O	I/O
P159	I/O	I/O	I/O
P160	I/O	I/O	I/O
P161	I/O	I/O	I/O
P162	I/O	I/O	I/O
P163	I/O	I/O	I/O
P164	I/O	I/O	I/O
P165	I/O	I/O	I/O
P166	I/O	I/O	I/O
P167	I/O	I/O	I/O
P168	I/O	I/O	I/O
P169	I/O	I/O	I/O
P170	I/O	I/O	I/O
P171	GND	GND	GND
P172	I/O	I/O	I/O
P173	I/O	I/O	I/O
P174	I/O	I/O	I/O
P175	I/O	I/O	I/O
P176	N.C.	N.C.	N.C.
P177	VCC	VCC	VCC
P178	I/O	I/O	I/O
P179	I/O	I/O	I/O
P180	I/O	I/O	I/O
P181	I/O	I/O	I/O
P182	I/O	I/O	I/O
P183	I/O	I/O	I/O
P184	I/O	I/O	I/O
P185	I/O	I/O	I/O
P186	I/O	I/O	I/O
P187	I/O	I/O	I/O
P188	I/O	I/O	I/O
P189	I/O	I/O	I/O
P190	GND	GND	GND
P191	VCC	VCC	VCC
P192	I/O ($\overline{INIT}$)	I/O ($\overline{INIT}$)	I/O ($\overline{INIT}$)
P193	I/O	I/O	I/O
P194	I/O	I/O	I/O
P195	I/O	I/O	I/O
P196	I/O	I/O	I/O
P197	I/O	I/O	I/O
P198	I/O	I/O	I/O
P199	I/O	I/O	I/O
P200	I/O	I/O	I/O
P201	I/O	I/O	I/O
P202	I/O	I/O	I/O
P203	I/O	I/O	I/O
P204	VCC	VCC	VCC
P205	N.C.	N.C.	N.C.
P206	I/O	I/O	I/O
P207	I/O	I/O	I/O

HQ304 Pin	XC4025E	XC4028EX XC4028XL	XC4036EX XC4036XL
P208	I/O	I/O	I/O
P209	I/O	I/O	I/O
P210	GND	GND	GND
P211	I/O	I/O	I/O
P212	I/O	I/O	I/O
P213	I/O	I/O	I/O
P214	I/O	I/O	I/O
P215	I/O	I/O	I/O
P216	I/O	I/O	I/O
P217	I/O	I/O	I/O
P218	I/O	I/O	I/O
P219	I/O	I/O	I/O
P220	I/O	I/O	I/O
P221	I/O ($\overline{LDC}$)	I/O ($\overline{LDC}$)	I/O ($\overline{LDC}$)
P222	I/O	I/O	I/O
P223	I/O	I/O	I/O
P224	I/O	I/O	I/O
P225	I/O (HDC)	I/O (HDC)	I/O (HDC)
P226	I/O, PGCK2	I/O, GCK3	I/O, GCK3
P227	I (M2)	I (M2)	I (M2)
P228	VCC	VCC	VCC
P229	I (M0)	I (M0)	I (M0)
P230	GND	GND	GND
P231	O (M1)	O (M1)	O (M1)
P232	I/O, SGCK2	I/O, GCK2	I/O, GCK2
P233	I/O	I/O	I/O
P234	I/O	I/O	I/O
P235	I/O	I/O	I/O
P236	I/O	I/O	I/O
P237	I/O	I/O	I/O
P238	I/O	I/O	I/O
P239	I/O	I/O	I/O
P240	I/O	I/O	I/O
P241	I/O	I/O	I/O
P242	I/O	I/O	I/O
P243	I/O	I/O	I/O
P244	I/O	I/O	I/O
P245	I/O	I/O	I/O
P246	I/O	I/O	I/O
P247	I/O	I/O	I/O
P248	GND	GND	GND
P249	I/O	I/O, FCLK2	I/O, FCLK2
P250	I/O	I/O	I/O
P251	I/O	I/O	I/O
P252	I/O	I/O	I/O
P253	VCC	VCC	VCC
P254	N.C.	N.C.	N.C.
P255	I/O	I/O	I/O
P256	I/O	I/O	I/O
P257	I/O	I/O	I/O
P258	I/O	I/O	I/O
P259	I/O	I/O	I/O
P260	I/O	I/O	I/O
P261	I/O	I/O	I/O
P262	I/O	I/O	I/O
P263	I/O	I/O	I/O
P264	I/O	I/O	I/O
P265	I/O	I/O	I/O
P266	I/O	I/O	I/O
P267	VCC	VCC	VCC
P268	GND	GND	GND
P269	I/O	I/O	I/O
P270	I/O	I/O	I/O
P271	I/O	I/O	I/O
P272	I/O	I/O	I/O
P273	I/O	I/O	I/O
P274	I/O	I/O	I/O
P275	I/O	I/O	I/O
P276	I/O	I/O	I/O
P277	I/O	I/O	I/O
P278	I/O	I/O	I/O
P279	I/O	I/O	I/O
P280	I/O	I/O	I/O
P281	N.C.	N.C.	N.C.
P282	VCC	VCC	VCC
P283	I/O	I/O	I/O
P284	I/O, TMS	I/O, TMS	I/O, TMS
P285	I/O	I/O	I/O
P286	I/O	I/O, FCLK1	I/O, FCLK1
P287	GND	GND	GND
P288	I/O	I/O	I/O
P289	I/O	I/O	I/O
P290	I/O	I/O	I/O
P291	I/O	I/O	I/O
P292	I/O	I/O	I/O
P293	I/O	I/O	I/O
P294	I/O	I/O	I/O
P295	I/O	I/O	I/O
P296	I/O	I/O	I/O
P297	I/O	I/O	I/O
P298	I/O, TCK	I/O, TCK	I/O, TCK
P299	I/O, TDI	I/O, TDI	I/O, TDI
P300	I/O	I/O	I/O
P301	I/O	I/O	I/O
P302	I/O (A17)	I/O (A17)	I/O (A17)
P303	I/O, PGCK1 (A16)	I/O, GCK1 (A16)	I/O, GCK1 (A16)
P304	GND	GND	GND

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Note: Shaded pins should be taken into account when designing PC boards, in case of future replacement by different devices.

BG352 Package Pinouts

BG352 Pin	XC4028EX/XL
AF1	GND
AF2	GND
AF3	I/O
AF4	I/O
AF5	GND
AF6	I/O
AF7	I/O
AF8	GND
AF9	I/O
AF10	VCC
AF11	I/O
AF12	I/O
AF13	GND
AF14	I/O ($\overline{\text{INIT}}$)
AF15	I/O
AF16	I/O
AF17	VCC
AF18	I/O
AF19	GND
AF20	I/O
AF21	I/O
AF22	GND
AF23	I/O
AF24	I/O
AF25	GND
AF26	GND
AE1	GND
AE2	VCC
AE3	I/O
AE4	N.C.
AE5	I/O
AE6	I/O
AE7	I/O
AE8	I/O
AE9	I/O
AE10	N.C.
AE11	I/O
AE12	I/O
AE13	I/O
AE14	I/O
AE15	I/O
AE16	I/O
AE17	I/O
AE18	I/O
AE19	I/O
AE20	I/O
AE21	I/O
AE22	I/O
AE23	I/O ($\overline{\text{LDC}}$)
AE24	I/O, GCK3
AE25	VCC
AE26	GND
AD1	I/O
AD2	I/O (D7)
AD3	DONE
AD4	I/O
AD5	I/O
AD6	I/O
AD7	I/O
AD8	I/O
AD9	I/O
AD10	I/O
AD11	I/O
AD12	I/O
AD13	I/O
AD14	I/O
AD15	I/O
AD16	N.C.
AD17	I/O
AD18	I/O
AD19	I/O
AD20	I/O
AD21	N.C.
AD22	I/O
AD23	I/O (HDC)
AD24	I (M0)
AD25	I/O
AD26	N.C.
AC1	I/O
AC2	N.C.
AC3	I/O, GCK5
AC4	$\overline{\text{PROGRAM}}$
AC5	I/O, GCK4
AC6	N.C.
AC7	I/O
AC8	VCC
AC9	I/O
AC10	I/O
AC11	N.C.
AC12	I/O
AC13	I/O
AC14	VCC
AC15	I/O
AC16	N.C.
AC17	I/O
AC18	I/O
AC19	I/O
AC20	VCC
AC21	N.C.
AC22	I/O
AC23	I (M2)
AC24	I/O, GCK2
AC25	N.C.
AC26	I/O
AB1	GND
AB2	I/O
AB3	N.C.
AB4	I/O
AB23	O (M1)
AB24	I/O
AB25	I/O
AB26	GND
AA1	I/O
AA2	I/O
AA3	I/O
AA4	I/O
AA23	I/O
AA24	I/O

BG352 Pin	XC4028EX/XL
AA25	I/O
AA26	I/O
Y1	I/O
Y2	I/O
Y3	I/O (D6)
Y4	VCC
Y23	I/O
Y24	I/O
Y25	I/O
Y26	I/O
W1	GND
W2	I/O
W3	I/O
W4	I/O
W23	VCC
W24	I/O
W25	I/O
W26	GND
V1	I/O ($\overline{CS0}$)
V2	I/O (D5)
V3	I/O
V4	I/O
V23	I/O
V24	I/O
V25	I/O
V26	I/O
U1	VCC
U2	I/O
U3	I/O
U4	I/O, FCLK3
U23	I/O, FCLK2
U24	I/O
U25	N.C.
U26	VCC
T1	I/O
T2	I/O
T3	N.C.
T4	N.C.
T23	I/O
T24	N.C.
T25	I/O
T26	I/O
R1	I/O
R2	I/O
R3	I/O
R4	I/O
R23	I/O
R24	I/O
R25	I/O
R26	I/O
P1	I/O
P2	I/O (D4)
P3	I/O
P4	VCC
P23	I/O
P24	I/O
P25	I/O
P26	GND
N1	GND
N2	I/O (D3)

BG352 Pin	XC4028EX/XL
N3	I/O
N4	I/O ($\overline{RS}$)
N23	VCC
N24	I/O
N25	I/O
N26	I/O
M1	I/O
M2	I/O
M3	I/O
M4	I/O
M23	I/O
M24	I/O
M25	I/O
M26	I/O
L1	I/O
L2	I/O
L3	I/O
L4	N.C.
L23	N.C.
L24	I/O
L25	I/O
L26	I/O
K1	VCC
K2	N.C.
K3	I/O
K4	I/O
K23	I/O
K24	I/O
K25	I/O
K26	VCC
J1	I/O (D2)
J2	I/O
J3	I/O, FCLK4
J4	I/O
J23	I/O, FCLK1
J24	I/O
J25	I/O
J26	N.C.
H1	GND
H2	I/O
H3	I/O
H4	VCC
H23	I/O
H24	I/O
H25	I/O, TMS
H26	GND
G1	I/O
G2	I/O
G3	I/O
G4	I/O (RCLK, $\overline{RDY/BUSY}$)
G23	VCC
G24	I/O
G25	I/O
G26	I/O
F1	I/O
F2	I/O
F3	I/O (D1)
F4	I/O
F23	N.C.
F24	I/O

BG352 Pin	XC4028EX/XL
F25	I/O
F26	I/O
E1	GND
E2	I/O
E3	I/O
E4	I/O, GCK6 (DOUT)
E23	I/O
E24	I/O, TCK
E25	I/O
E26	GND
D1	N.C.
D2	I/O
D3	I/O (D0, DIN)
D4	O (TDO)
D5	I/O
D6	I/O (CS1, A2)
D7	VCC
D8	I/O
D9	I/O
D10	I/O
D11	I/O
D12	I/O (A4)
D13	VCC
D14	I/O (A8)
D15	I/O
D16	N.C.
D17	I/O
D18	I/O
D19	VCC
D20	I/O
D21	I/O
D22	I/O (A14)
D23	I/O, GCK1 (A16)
D24	I/O
D25	N.C.
D26	I/O
C1	N.C.
C2	I/O
C3	CCLK
C4	I/O, GCK7 (A1)
C5	N.C.
C6	I/O (A3)
C7	I/O
C8	N.C.
C9	I/O
C10	I/O
C11	N.C.
C12	I/O (A5)
C13	I/O (A21)
C14	I/O (A9)
C15	I/O
C16	I/O
C17	I/O
C18	I/O
C19	I/O
C20	I/O
C21	I/O (A13)
C22	I/O
C23	I/O
C24	I/O, GCK8 (A15)

BG352 Pin	XC4028EX/XL
C25	I/O (A17)
C26	I/O, TDI
B1	GND
B2	VCC
B3	I/O (A0, $\overline{WS}$)
B4	N.C.
B5	I/O
B6	I/O
B7	I/O
B8	I/O
B9	I/O
B10	N.C.
B11	I/O
B12	I/O
B13	I/O (A20)
B14	I/O (A7)
B15	I/O (A18)
B16	I/O (A11)
B17	I/O
B18	I/O
B19	I/O
B20	I/O
B21	I/O
B22	I/O (A12)
B23	N.C.
B24	I/O
B25	VCC
B26	GND
A1	GND
A2	GND
A3	I/O
A4	I/O
A5	GND
A6	I/O
A7	I/O
A8	GND
A9	I/O
A10	VCC
A11	I/O
A12	I/O
A13	I/O (A6)
A14	GND
A15	I/O (A19)
A16	I/O (A10)
A17	VCC
A18	N.C.
A19	GND
A20	I/O
A21	I/O
A22	GND
A23	I/O
A24	N.C.
A25	GND
A26	GND

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Note: Viewed from the bottom side, the package pins start at the top row and go from the left edge to the right edge. Viewed from the top side, the pins start at the top row and go from the right edge to the left edge.

PG411 Package Pinouts

PG411 Pin	XC4036EX/XL	XC4044EX/XL
AW1	I/O	I/O
AW3	GND	GND
AW5	I/O	I/O
AW7	I/O ($\overline{RCLK}$, RDY/$\overline{BUSY}$)	I/O ($\overline{RCLK}$, RDY/$\overline{BUSY}$)
AW9	VCC	VCC
AW11	GND	GND
AW13	I/O	I/O
AW15	**N.C.**	**I/O**
AW17	I/O	I/O
AW19	VCC	VCC
AW21	GND	GND
AW23	**N.C.**	**I/O**
AW25	**N.C.**	**I/O**
AW27	I/O	I/O
AW29	VCC	VCC
AW31	GND	GND
AW33	I/O	I/O
AW35	N.C.	N.C.
AW37	VCC	VCC
AW39	I/O	I/O
AV2	I/O, GCK7 (A1)	I/O, GCK7 (A1)
AV4	I/O	I/O
AV6	I/O	I/O
AV8	**N.C.**	**I/O**
AV10	I/O	I/O
AV12	I/O	I/O
AV14	I/O	I/O
AV16	I/O	I/O
AV18	I/O	I/O
AV20	I/O ($\overline{RS}$)	I/O ($\overline{RS}$)
AV22	I/O	I/O
AV24	I/O	I/O
AV26	N.C.	N.C.
AV28	I/O	I/O
AV30	I/O	I/O
AV32	I/O (D6)	I/O (D6)
AV34	N.C.	N.C.
AV36	I/O	I/O
AV38	I/O	I/O
AU1	VCC	VCC
AU3	I/O, GCK6 (DOUT)	I/O, GCK6 (DOUT)
AU5	N.C.	N.C.
AU7	I/O (D1)	I/O (D1)
AU9	**N.C.**	**I/O**
AU11	I/O	I/O
AU13	N.C.	N.C.
AU15	N.C.	N.C.
AU17	**N.C.**	**I/O**
AU19	I/O (D3)	I/O (D3)
AU21	I/O	I/O
AU23	I/O	I/O
AU25	N.C.	N.C.
AU27	I/O ($\overline{CS0}$)	I/O ($\overline{CS0}$)
AU29	I/O	I/O
AU31	I/O	I/O
AU33	I/O	I/O
AU35	I/O	I/O
AU37	N.C.	N.C.
AU39	GND	GND
AT2	N.C.	N.C.
AT4	I/O (A0, $\overline{WS}$)	I/O (A0, $\overline{WS}$)
AT6	GND	GND
AT8	I/O	I/O
AT10	I/O	I/O
AT12	I/O	I/O
AT14	GND	GND
AT16	I/O	I/O
AT18	I/O	I/O
AT20	GND	GND
AT22	I/O	I/O
AT24	I/O	I/O
AT26	GND	GND
AT28	I/O, FCLK3	I/O, FCLK3
AT30	**N.C.**	**I/O**
AT32	I/O	I/O
AT34	VCC	VCC
AT36	I/O, GCK4	I/O, GCK4
AT38	I/O	I/O
AR1	I/O	I/O
AR3	I/O	I/O
AR5	CCLK	CCLK
AR7	I/O	I/O
AR9	I/O	I/O
AR11	I/O	I/O
AR13	I/O, FCLK4	I/O, FCLK4
AR15	I/O (D2)	I/O (D2)
AR17	I/O	I/O
AR19	I/O	I/O
AR21	I/O	I/O
AR23	I/O	I/O
AR25	I/O	I/O
AR27	I/O	I/O
AR29	I/O	I/O
AR31	I/O	I/O
AR33	I/O	I/O
AR35	DONE	DONE
AR37	N.C.	N.C.
AR39	I/O	I/O
AP2	I/O	I/O
AP4	VCC	VCC
AP6	I/O (D0, DIN)	I/O (D0, DIN)
AP8	N.C.	N.C.
AP10	I/O	I/O
AP12	I/O	I/O

PG411 Pin	XC4036EX/XL	XC4044EX/XL
AP14	I/O	I/O
AP16	I/O	I/O
AP18	I/O	I/O
AP20	I/O (D4)	I/O (D4)
AP22	I/O	I/O
AP24	I/O (D5)	I/O (D5)
AP26	I/O	I/O
AP28	I/O	I/O
AP30	**N.C.**	**I/O**
AP32	I/O	I/O
AP34	I/O, GCK5	I/O, GCK5
AP36	GND	GND
AP38	**N.C.**	**I/O**
AN1	**N.C.**	**I/O**
AN3	I/O (A3)	I/O (A3)
AN5	N.C.	N.C.
AN7	O, TDO	O, TDO
AN9	I/O	I/O
AN31	I/O	I/O
AN33	$\overline{\text{PROGRAM}}$	$\overline{\text{PROGRAM}}$
AN35	I/O	I/O
AN37	I/O	I/O
AN39	I/O	I/O
AM2	I/O	I/O
AM4	I/O	I/O
AM6	I/O	I/O
AM8	I/O	I/O
AM32	I/O (D7)	I/O (D7)
AM34	I/O	I/O
AM36	I/O	I/O
AM38	I/O	I/O
AL1	GND	GND
AL3	I/O	I/O
AL5	I/O	I/O
AL7	I/O	I/O
AL33	I/O	I/O
AL35	N.C.	N.C.
AL37	I/O	I/O
AL39	VCC	VCC
AK2	**N.C.**	**I/O**
AK4	I/O	I/O
AK6	I/O (CS1, A2)	I/O (CS1, A2)
AK34	I/O	I/O
AK36	I/O	I/O
AK38	**N.C.**	**I/O**
AJ1	VCC	VCC
AJ3	I/O	I/O
AJ5	N.C.	N.C.
AJ35	I/O	I/O
AJ37	I/O	I/O
AJ39	GND	GND
AH2	I/O	I/O
AH4	I/O	I/O

PG411 Pin	XC4036EX/XL	XC4044EX/XL
AH6	I/O	I/O
AH34	I/O	I/O
AH36	I/O	I/O
AH38	I/O	I/O
AG1	I/O	I/O
AG3	I/O	I/O
AG5	I/O	I/O
AG35	I/O	I/O
AG37	I/O	I/O
AG39	I/O	I/O
AF2	N.C.	N.C.
AF4	GND	GND
AF6	I/O	I/O
AF34	I/O	I/O
AF36	GND	GND
AF38	N.C.	N.C.
AE1	I/O	I/O
AE3	I/O	I/O
AE5	I/O	I/O
AE35	I/O	I/O
AE37	I/O	I/O
AE39	I/O	I/O
AD2	I/O (A4)	I/O (A4)
AD4	I/O (A21)	I/O (A21)
AD6	I/O	I/O
AD34	I/O	I/O
AD36	I/O	I/O
AD38	I/O	I/O
AC1	I/O	I/O
AC3	**N.C.**	**I/O**
AC5	I/O	I/O
AC35	I/O	I/O
AC37	I/O	I/O
AC39	**N.C.**	**I/O**
AB2	**N.C.**	**I/O**
AB4	I/O (A5)	I/O (A5)
AB6	I/O	I/O
AB34	I/O	I/O
AB36	I/O	I/O
AB38	I/O	I/O
AA1	GND	GND
AA3	I/O (A6)	I/O (A6)
AA5	I/O (A20)	I/O (A20)
AA35	I/O	I/O
AA37	**N.C.**	**I/O**
AA39	VCC	VCC
Y2	I/O (A9)	I/O (A9)
Y4	GND	GND
Y6	I/O (A7)	I/O (A7)
Y34	I/O	I/O
Y36	GND	GND
Y38	**N.C.**	**I/O**
W1	VCC	VCC

PG411 Pin	XC4036EX/XL	XC4044EX/XL
W3	I/O (A8)	I/O (A8)
W5	**N.C.**	**I/O**
W35	**N.C.**	**I/O**
W37	I/O ($\overline{INIT}$)	I/O ($\overline{INIT}$)
W39	GND	GND
V2	**N.C.**	**I/O**
V4	I/O (A19)	I/O (A19)
V6	I/O	I/O
V34	I/O	I/O
V36	I/O	I/O
V38	I/O	I/O
U1	I/O	I/O
U3	I/O (A10)	I/O (A10)
U5	I/O	I/O
U35	I/O	I/O
U37	I/O	I/O
U39	I/O	I/O
T2	I/O (A18)	I/O (A18)
T4	I/O	I/O
T6	I/O	I/O
T34	I/O	I/O
T36	I/O	I/O
T38	I/O	I/O
R1	I/O (A11)	I/O (A11)
R3	N.C.	N.C.
R5	I/O	I/O
R35	I/O	I/O
R37	I/O	I/O
R39	I/O	I/O
P2	I/O	I/O
P4	GND	GND
P6	I/O	I/O
P34	I/O	I/O
P36	GND	GND
P38	N.C.	N.C.
N1	I/O	I/O
N3	N.C.	N.C.
N5	I/O	I/O
N35	I/O	I/O
N37	I/O	I/O
N39	I/O	I/O
M2	I/O	I/O
M4	I/O	I/O
M6	I/O	I/O
M34	I/O	I/O
M36	I/O	I/O
M38	I/O	I/O
L1	GND	GND
L3	I/O	I/O
L5	**N.C.**	**I/O**
L35	N.C.	N.C.
L37	I/O	I/O
L39	VCC	VCC

PG411 Pin	XC4036EX/XL	XC4044EX/XL
K2	I/O	I/O
K4	I/O	I/O
K6	I/O	I/O
K34	I/O	I/O
K36	**N.C.**	**I/O**
K38	**N.C.**	**I/O**
J1	VCC	VCC
J3	I/O	I/O
J5	**N.C.**	**I/O**
J7	I/O	I/O
J33	I/O	I/O
J35	I/O	I/O
J37	I/O	I/O
J39	GND	GND
H2	I/O	I/O
H4	I/O (A12)	I/O (A12)
H6	I/O	I/O
H8	I/O, GCK1 (A16)	I/O, GCK1 (A16)
H32	I/O	I/O
H34	N.C.	N.C.
H36	I/O	I/O
H38	I/O	I/O
G1	I/O	I/O
G3	I/O (A13)	I/O (A13)
G5	N.C.	N.C.
G7	I/O, GCK8 (A15)	I/O, GCK8 (A15)
G9	I/O, TCK	I/O, TCK
G31	I/O	I/O
G33	I (M2)	I (M2)
G35	I/O ($\overline{LDC}$)	I/O ($\overline{LDC}$)
G37	I/O	I/O
G39	I/O	I/O
F2	N.C.	N.C.
F4	GND	GND
F6	I/O (A17)	I/O (A17)
F8	I/O	I/O
F10	I/O	I/O
F12	I/O	I/O
F14	I/O	I/O
F16	I/O	I/O
F18	**N.C.**	**I/O**
F20	I/O	I/O
F22	**N.C.**	**I/O**
F24	I/O	I/O
F26	I/O	I/O
F28	I/O	I/O
F30	I/O	I/O
F32	I/O	I/O
F34	I/O	I/O
F36	VCC	VCC
F38	I/O	I/O
E1	I/O	I/O
E3	I/O	I/O

PG411 Pin	XC4036EX/XL	XC4044EX/XL
E5	I/O (A14)	I/O (A14)
E7	N.C.	N.C.
E9	I/O	I/O
E11	I/O, TMS	I/O, TMS
E13	I/O	I/O
E15	I/O	I/O
E17	I/O	I/O
E19	I/O	I/O
E21	I/O	I/O
E23	N.C.	N.C.
E25	I/O	I/O
E27	I/O	I/O
E29	I/O	I/O
E31	I/O	I/O
E33	I/O	I/O
E35	I (M0)	I (M0)
E37	N.C.	N.C.
E39	I/O	I/O
D2	I/O	I/O
D4	I/O	I/O
D6	VCC	VCC
D8	**N.C.**	**I/O**
D10	I/O	I/O
D12	N.C.	N.C.
D14	GND	GND
D16	I/O	I/O
D18	I/O	I/O
D20	GND	GND
D22	I/O	I/O
D24	I/O	I/O
D26	GND	GND
D28	I/O	I/O
D30	**N.C.**	**I/O**
D32	**N.C.**	**I/O**
D34	GND	GND
D36	I/O, GCK3	I/O, GCK3
D38	I/O	I/O
C1	GND	GND
C3	I/O	I/O
C5	I/O	I/O
C7	**N.C.**	**I/O**
C9	I/O	I/O
C11	I/O, FCLK1	I/O, FCLK1
C13	I/O	I/O
C15	**N.C.**	**I/O**
C17	I/O	I/O
C19	I/O	I/O
C21	I/O	I/O
C23	**N.C.**	**I/O**
C25	N.C.	N.C.
C27	I/O	I/O
C29	I/O, FCLK2	I/O, FCLK2
C31	I/O	I/O

PG411 Pin	XC4036EX/XL	XC4044EX/XL
C33	N.C.	N.C.
C35	I/O	I/O
C37	I/O (HDC)	I/O (HDC)
C39	VCC	VCC
B2	I/O, TDI	I/O, TDI
B4	I/O	I/O
B6	N.C.	N.C.
B8	I/O	I/O
B10	I/O	I/O
B12	I/O	I/O
B14	I/O	I/O
B16	I/O	I/O
B18	I/O	I/O
B20	I/O	I/O
B22	I/O	I/O
B24	I/O	I/O
B26	I/O	I/O
B28	I/O	I/O
B30	I/O	I/O
B32	I/O	I/O
B34	N.C.	N.C.
B36	I/O, GCK2	I/O, GCK2
B38	I/O	I/O
A3	VCC	VCC
A5	I/O	I/O
A7	I/O	I/O
A9	GND	GND
A11	VCC	VCC
A13	N.C.	N.C.
A15	I/O	I/O
A17	I/O	I/O
A19	GND	GND
A21	VCC	VCC
A23	I/O	I/O
A25	I/O	I/O
A27	I/O	I/O
A29	GND	GND
A31	VCC	VCC
A33	I/O	I/O
A35	I/O	I/O
A37	GND	GND
A39	O (M1)	O (M1)

3/26/96

Note: Shaded pins should be taken into account when designing PC boards, in case of future replacement by different devices.

Note: Viewed from the bottom side, the package pins start at the top row and go from the left edge to the right edge. Viewed from the top side, the pins start at the top row and go from the right edge to the left edge.

BG432 Package Pinouts

BG432 Pin	XC4036EX XC4036XL	XC4044EX XC4044XL	XC4052XL
AL1	VCC	VCC	VCC
AL2	GND	GND	GND
AL3	GND	GND	GND
AL4	I/O	I/O	I/O
AL5	I/O	I/O	I/O
AL6	I/O	I/O	I/O
AL7	GND	GND	GND
AL8	I/O	I/O	I/O
AL9	GND	GND	GND
AL10	I/O	I/O	I/O
AL11	VCC	VCC	VCC
AL12	I/O	I/O	I/O
AL13	I/O	I/O	I/O
AL14	GND	GND	GND
AL15	**N.C.**	**I/O**	**I/O**
AL16	I/O	I/O	I/O
AL17	**N.C.**	**I/O**	**I/O**
AL18	GND	GND	GND
AL19	I/O	I/O	I/O
AL20	I/O	I/O	I/O
AL21	VCC	VCC	VCC
AL22	I/O	I/O	I/O
AL23	GND	GND	GND
AL24	I/O	I/O	I/O
AL25	GND	GND	GND
AL26	I/O	I/O	I/O
AL27	I/O	I/O	I/O
AL28	I/O	I/O	I/O
AL29	GND	GND	GND
AL30	GND	GND	GND
AL31	VCC	VCC	VCC
AK1	GND	GND	GND
AK2	GND	GND	GND
AK3	I/O	I/O	I/O
AK4	I/O	I/O	I/O
AK5	I/O	I/O	I/O
AK6	I/O	I/O	I/O
AK7	I/O	I/O	I/O
AK8	I/O	I/O	I/O
AK9	I/O	I/O	I/O
AK10	I/O	I/O	I/O
AK11	**N.C.**	**N.C.**	**I/O**
AK12	I/O	I/O	I/O
AK13	I/O	I/O	I/O
AK14	I/0	I/O	I/O
AK15	I/O	I/O	I/O
AK16	I/O ($\overline{\text{INIT}}$)	I/O ($\overline{\text{INIT}}$)	I/O ($\overline{\text{INIT}}$)
AK17	**N.C.**	**I/O**	**I/O**
AK18	I/O	I/O	I/O
AK19	I/O	I/O	I/O
AK20	I/O	I/O	I/O
AK21	I/O	I/O	I/O
AK22	I/O	I/O	I/O
AK23	I/O	I/O	I/O
AK24	**N.C.**	**I/O**	**I/O**
AK25	I/O	I/O	I/O
AK26	I/O	I/O	I/O
AK27	**N.C.**	**N.C.**	**I/O**
AK28	I/O	I/O	I/O
AK29	I/O, GCK3	I/O, GCK3	I/O, GCK3
AK30	GND	GND	GND
AK31	GND	GND	GND
AJ1	GND	GND	GND
AJ2	I/O (D7)	I/O (D7)	I/O (D7)
AJ3	VCC	VCC	VCC
AJ4	I/O, GCK4	I/O, GCK4	I/O, GCK4
AJ5	**N.C.**	**N.C.**	**I/O**
AJ6	I/O	I/O	I/O
AJ7	I/O	I/O	I/O
AJ8	**N.C.**	**I/O**	**I/O**
AJ9	I/O	I/O	I/O
AJ10	I/O	I/O	I/O
AJ11	I/O	I/O	I/O
AJ12	**N.C.**	**N.C.**	**I/O**
AJ13	I/O	I/O	I/O
AJ14	I/O	I/O	I/O
AJ15	**N.C.**	**I/O**	**I/O**
AJ16	I/O	I/O	I/O
AJ17	I/O	I/O	I/O
AJ18	I/O	I/O	I/O
AJ19	I/O	I/O	I/O
AJ20	**N.C.**	**N.C.**	**I/O**
AJ21	I/O	I/O	I/O
AJ22	I/O	I/O	I/O
AJ23	I/O	I/O	I/O
AJ24	I/O	I/O	I/O
AJ25	I/O	I/O	I/O
AJ26	**N.C.**	**N.C.**	**I/O**
AJ27	I/O	I/O	I/O
AJ28	I (M2)	I (M2)	I (M2)
AJ29	VCC	VCC	VCC
AJ30	I/O, GCK2	I/O, GCK2	I/O, GCK2
AJ31	GND	GND	GND
AH1	I/O	I/O	I/O
AH2	I/O	I/O	I/O
AH3	$\overline{\text{PROGRAM}}$	$\overline{\text{PROGRAM}}$	$\overline{\text{PROGRAM}}$
AH4	DONE	DONE	DONE
AH5	I/O	I/O	I/O
AH6	**N.C.**	**N.C.**	**I/O**
AH7	I/O	I/O	I/O
AH8	I/O	I/O	I/O
AH9	**N.C.**	**I/O**	**I/O**
AH10	I/O	I/O	I/O
AH11	VCC	VCC	VCC
AH12	I/O	I/O	I/O
AH13	I/O	I/O	I/O
AH14	I/O	I/O	I/O
AH15	I/O	I/O	I/O
AH16	GND	GND	GND
AH17	I/O	I/O	I/O

BG432 Pin	XC4036EX XC4036XL	XC4044EX XC4044XL	XC4052XL
AH18	I/O	I/O	I/O
AH19	**N.C.**	**N.C.**	**I/O**
AH20	I/O	I/O	I/O
AH21	VCC	VCC	VCC
AH22	I/O	I/O	I/O
AH23	**N.C.**	**I/O**	**I/O**
AH24	I/O	I/O	I/O
AH25	I/O	I/O	I/O
AH26	I/O ($\overline{LDC}$)	I/O ($\overline{LDC}$)	I/O ($\overline{LDC}$)
AH27	I/O (HDC)	I/O (HDC)	I/O (HDC)
AH28	I (M0)	I (M0)	I (M0)
AH29	O (M1)	O (M1)	O (M1)
AH30	I/O	I/O	I/O
AH31	I/O	I/O	I/O
AG1	**N.C.**	**N.C.**	**I/O**
AG2	I/O	I/O	I/O
AG3	I/O	I/O	I/O
AG4	I/O, GCK5	I/O, GCK5	I/O, GCK5
AG28	I/O	I/O	I/O
AG29	I/O	I/O	I/O
AG30	I/O	I/O	I/O
AG31	I/O	I/O	I/O
AF1	I/O (D6)	I/O (D6)	I/O (D6)
AF2	I/O	I/O	I/O
AF3	I/O	I/O	I/O
AF4	I/O	I/O	I/O
AF28	I/O	I/O	I/O
AF29	**N.C.**	**N.C.**	**I/O**
AF30	**N.C.**	**N.C.**	**I/O**
AF31	I/O	I/O	I/O
AE1	GND	GND	GND
AE2	I/O	I/O	I/O
AE3	I/O	I/O	I/O
AE4	**N.C.**	**N.C.**	**I/O**
AE28	I/O	I/O	I/O
AE29	I/O	I/O	I/O
AE30	I/O	I/O	I/O
AE31	GND	GND	GND
AD1	I/O	I/O	I/O
AD2	**N.C.**	**I/O**	**I/O**
AD3	I/O	I/O	I/O
AD4	I/O	I/O	I/O
AD28	I/O	I/O	I/O
AD29	I/O	I/O	I/O
AD30	**N.C.**	**I/O**	**I/O**
AD31	**N.C.**	**I/O**	**I/O**
AC1	GND	GND	GND
AC2	I/O	I/O	I/O
AC3	I/O	I/O	I/O
AC4	**N.C.**	**I/O**	**I/O**
AC28	I/O	I/O	I/O
AC29	I/O	I/O	I/O
AC30	I/O	I/O	I/O
AC31	GND	GND	GND
AB1	I/O, FCLK3	I/O, FCLK3	I/O, FCLK3
AB2	I/O	I/O	I/O

BG432 Pin	XC4036EX XC4036XL	XC4044EX XC4044XL	XC4052XL
AB3	I/O	I/O	I/O
AB4	I/O	I/O	I/O
AB28	I/O	I/O	I/O
AB29	I/O, FCLK2	I/O, FCLK2	I/O, FCLK2
AB30	I/O	I/O	I/O
AB31	I/O	I/O	I/O
AA1	VCC	VCC	VCC
AA2	I/O (D5)	I/O (D5)	I/O (D5)
AA3	I/O	I/O	I/O
AA4	VCC	VCC	VCC
AA28	VCC	VCC	VCC
AA29	I/O	I/O	I/O
AA30	I/O	I/O	I/O
AA31	VCC	VCC	VCC
Y1	**N.C.**	**N.C.**	**I/O**
Y2	I/O ($\overline{CS0}$)	I/O ($\overline{CS0}$)	I/O ($\overline{CS0}$)
Y3	I/O	I/O	I/O
Y4	I/O	I/O	I/O
Y28	I/O	I/O	I/O
Y29	I/O	I/O	I/O
Y30	I/O	I/O	I/O
Y31	**N.C.**	**N.C.**	**I/O**
W1	**N.C.**	**N.C.**	**I/O**
W2	**N.C.**	**I/O**	**I/O**
W3	I/O	I/O	I/O
W4	I/O	I/O	I/O
W28	**N.C.**	**N.C.**	**I/O**
W29	I/O	I/O	I/O
W30	I/O	I/O	I/O
W31	**N.C.**	**I/O**	**I/O**
V1	GND	GND	GND
V2	**N.C.**	**I/O**	**I/O**
V3	I/O	I/O	I/O
V4	I/O	I/O	I/O
V28	**N.C.**	**I/O**	**I/O**
V29	I/O	I/O	I/O
V30	I/O	I/O	I/O
V31	GND	GND	GND
U1	I/O	I/O	I/O
U2	I/O	I/O	I/O
U3	I/O	I/O	I/O
U4	I/O	I/O	I/O
U28	I/O	I/O	I/O
U29	I/O	I/O	I/O
U30	I/O	I/O	I/O
U31	I/O	I/O	I/O
T1	I/O (D4)	I/O (D4)	I/O (D4)
T2	I/O	I/O	I/O
T3	I/O (D3)	I/O (D3)	I/O (D3)
T4	GND	GND	GND
T28	GND	GND	GND
T29	I/O	I/O	I/O
T30	I/O	I/O	I/O
T31	I/O	I/O	I/O
R1	I/O ($\overline{RS}$)	I/O ($\overline{RS}$)	I/O ($\overline{RS}$)
R2	I/O	I/O	I/O

BG432 Pin	XC4036EX XC4036XL	XC4044EX XC4044XL	XC4052XL
R3	I/O	I/O	I/O
R4	I/O	I/O	I/O
R28	I/O	I/O	I/O
R29	I/O	I/O	I/O
R30	I/O	I/O	I/O
R31	I/O	I/O	I/O
P1	GND	GND	GND
P2	I/O	I/O	I/O
P3	I/O	I/O	I/O
P4	I/O	I/O	I/O
P28	I/O	I/O	I/O
P29	I/O	I/O	I/O
P30	I/O	I/O	I/O
P31	GND	GND	GND
N1	**N.C.**	**I/O**	**I/O**
N2	**N.C.**	**I/O**	**I/O**
N3	I/O	I/O	I/O
N4	I/O	I/O	I/O
N28	I/O	I/O	I/O
N29	**N.C.**	**I/O**	**I/O**
N30	**N.C.**	**I/O**	**I/O**
N31	I/O	I/O	I/O
M1	I/O	I/O	I/O
M2	I/O	I/O	I/O
M3	**N.C.**	**N.C.**	**I/O**
M4	**N.C.**	**N.C.**	**I/O**
M28	**N.C.**	**N.C.**	**I/O**
M29	I/O	I/O	I/O
M30	**N.C.**	**N.C.**	**I/O**
M31	I/O	I/O	I/O
L1	VCC	VCC	VCC
L2	I/O (D2)	I/O (D2)	I/O (D2)
L3	I/O	I/O	I/O
L4	VCC	VCC	VCC
L28	VCC	VCC	VCC
L29	I/O	I/O	I/O
L30	I/O	I/O	I/O
L31	VCC	VCC	VCC
K1	I/O	I/O	I/O
K2	I/O, FCLK4	I/O, FCLK4	I/O, FCLK4
K3	I/O	I/O	I/O
K4	I/O	I/O	I/O
K28	I/O, FCLK1	I/O, FCLK1	I/O, FCLK1
K29	I/O	I/O	I/O
K30	I/O, TMS	I/O, TMS	I/O, TMS
K31	I/O	I/O	I/O
J1	GND	GND	GND
J2	I/O	I/O	I/O
J3	I/O	I/O	I/O
J4	I/O	I/O	I/O
J28	I/O	I/O	I/O
J29	I/O	I/O	I/O
J30	I/O	I/O	I/O
J31	GND	GND	GND
H1	I/O	I/O	I/O
H2	I/O	I/O	I/O

BG432 Pin	XC4036EX XC4036XL	XC4044EX XC4044XL	XC4052XL
H3	I/O	I/O	I/O
H4	I/O	I/O	I/O
H28	I/O	I/O	I/O
H29	I/O	I/O	I/O
H30	I/O	I/O	I/O
H31	I/O	I/O	I/O
G1	GND	GND	GND
G2	I/O	I/O	I/O
G3	**N.C.**	**I/O**	**I/O**
G4	I/O (D1)	I/O (D1)	I/O (D1)
G28	I/O	I/O	I/O
G29	I/O	I/O	I/O
G30	I/O	I/O	I/O
G31	GND	GND	GND
F1	**N.C.**	**I/O**	**I/O**
F2	I/O ($\overline{\text{RCLK}}$, RDY/$\overline{\text{BUSY}}$)	I/O ($\overline{\text{RCLK}}$, RDY/$\overline{\text{BUSY}}$)	I/O ($\overline{\text{RCLK}}$, RDY/$\overline{\text{BUSY}}$)
F3	I/O	I/O	I/O
F4	**N.C.**	**N.C.**	**I/O**
F28	**N.C.**	**N.C.**	**I/O**
F29	**N.C.**	**N.C.**	**I/O**
F30	**N.C.**	**I/O**	**I/O**
F31	**N.C.**	**I/O**	**I/O**
E1	I/O	I/O	I/O
E2	**N.C.**	**N.C.**	**I/O**
E3	I/O	I/O	I/O
E4	I/O	I/O	I/O
E28	I/O	I/O	I/O
E29	I/O	I/O	I/O
E30	I/O	I/O	I/O
E31	I/O	I/O	I/O
D1	I/O	I/O	I/O
D2	I/O	I/O	I/O
D3	I/O, GCK6 (DOUT)	I/O, GCK6 (DOUT)	I/O, GCK6 (DOUT)
D4	CCLK	CCLK	CCLK
D5	I/O, GCK7 (A1)	I/O, GCK7 (A1)	I/O, GCK7 (A1)
D6	**N.C.**	**N.C.**	**I/O**
D7	I/O (A3)	I/O (A3)	I/O (A3)
D8	I/O	I/O	I/O
D9	I/O	I/O	I/O
D10	I/O	I/O	I/O
D11	VCC	VCC	VCC
D12	I/O	I/O	I/O
D13	**N.C.**	**N.C.**	**I/O**
D14	I/O	I/O	I/O
D15	I/O	I/O	I/O
D16	GND	GND	GND
D17	I/O (A8)	I/O (A8)	I/O (A8)
D18	I/O (A18)	I/O (A18)	I/O (A18)
D19	I/O	I/O	I/O
D20	**N.C.**	**N.C.**	**I/O**
D21	VCC	VCC	VCC
D22	I/O	I/O	I/O
D23	**N.C.**	**I/O**	**I/O**
D24	I/O (A12)	I/O (A12)	I/O (A12)

BG432 Pin	XC4036EX XC4036XL	XC4044EX XC4044XL	XC4052XL
D25	I/O	I/O	I/O
D26	**N.C.**	**N.C.**	**I/O**
D27	I/O	I/O	I/O
D28	I/O, GCK8 (A15)	I/O, GCK8 (A15)	I/O, GCK8 (A15)
D29	I/O, GCK1 (A16)	I/O, GCK1 (A16)	I/O, GCK1 (A16)
D30	I/O, TDI	I/O, TDI	I/O, TDI
D31	I/O, TCK	I/O, TCK	I/O, TCK
C1	GND	GND	GND
C2	I/O (D0, DIN)	I/O (D0, DIN)	I/O (D0, DIN)
C3	VCC	VCC	VCC
C4	O, TDO	O, TDO	O, TDO
C5	I/O	I/O	I/O
C6	I/O	I/O	I/O
C7	I/O	I/O	I/O
C8	N.C.	N.C.	N.C.
C9	I/O	I/O	I/O
C10	I/O	I/O	I/O
C11	I/O	I/O	I/O
C12	I/O	I/O	I/O
C13	I/O	I/O	I/O
C14	I/O (A4)	I/O (A4)	I/O (A4)
C15	I/O (A21)	I/O (A21)	I/O (A21)
C16	**N.C.**	**I/O**	**I/O**
C17	**N.C.**	**I/O**	**I/O**
C18	I/O (A19)	I/O (A19)	I/O (A19)
C19	I/O (A11)	I/O (A11)	I/O (A11)
C20	I/O	I/O	I/O
C21	I/O	I/O	I/O
C22	I/O	I/O	I/O
C23	I/O	I/O	I/O
C24	I/O	I/O	I/O
C25	I/O	I/O	I/O
C26	I/O	I/O	I/O
C27	I/O	I/O	I/O
C28	I/O (A14)	I/O (A14)	I/O (A14)
C29	VCC	VCC	VCC
C30	I/O (A17)	I/O (A17)	I/O (A17)
C31	GND	GND	GND
B1	GND	GND	GND
B2	GND	GND	GND
B3	I/O (A0, $\overline{WS}$)	I/O (A0, $\overline{WS}$)	I/O (A0, $\overline{WS}$)
B4	I/O	I/O	I/O
B5	I/O	I/O	I/O
B6	I/O	I/O	I/O
B7	I/O	I/O	I/O
B8	**N.C.**	**I/O**	**I/O**
B9	I/O	I/O	I/O
B10	I/O	I/O	I/O
B11	I/O	I/O	I/O
B12	**N.C.**	**N.C.**	**I/O**
B13	I/O	I/O	I/O
B14	I/O	I/O	I/O
B15	I/O (A20)	I/O (A20)	I/O (A20)
B16	I/O (A6)	I/O (A6)	I/O (A6)
B17	**N.C.**	**I/O**	**I/O**
B18	I/O	I/O	I/O

BG432 Pin	XC4036EX XC4036XL	XC4044EX XC4044XL	XC4052XL
B19	I/O (A10)	I/O (A10)	I/O (A10)
B20	I/O	I/O	I/O
B21	**N.C.**	**N.C.**	**I/O**
B22	I/O	I/O	I/O
B23	I/O	I/O	I/O
B24	I/O	I/O	I/O
B25	**N.C.**	**I/O**	**I/O**
B26	I/O (A13)	I/O (A13)	I/O (A13)
B27	I/O	I/O	I/O
B28	I/O	I/O	I/O
B29	I/O	I/O	I/O
B30	GND	GND	GND
B31	GND	GND	GND
A1	VCC	VCC	VCC
A2	GND	GND	GND
A3	GND	GND	GND
A4	**N.C.**	**N.C.**	**I/O**
A5	I/O (CS1, A2)	I/O (CS1, A2)	I/O (CS1, A2)
A6	I/O	I/O	I/O
A7	GND	GND	GND
A8	**N.C.**	**I/O**	**I/O**
A9	GND	GND	GND
A10	I/O	I/O	I/O
A11	VCC	VCC	VCC
A12	I/O	I/O	I/O
A13	I/O (A5)	I/O (A5)	I/O (A5)
A14	GND	GND	GND
A15	**N.C.**	**I/O**	**I/O**
A16	I/O (A7)	I/O (A7)	I/O (A7)
A17	I/O (A9)	I/O (A9)	I/O (A9)
A18	GND	GND	GND
A19	I/O	I/O	I/O
A20	I/O	I/O	I/O
A21	VCC	VCC	VCC
A22	I/O	I/O	I/O
A23	GND	GND	GND
A24	I/O	I/O	I/O
A25	GND	GND	GND
A26	I/O	I/O	I/O
A27	I/O	I/O	I/O
A28	**N.C.**	**N.C.**	**I/O**
A29	GND	GND	GND
A30	GND	GND	GND
A31	VCC	VCC	VCC

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Note: Shaded pins should be taken into account when designing PC boards, in case of future replacement by different devices.

Note: Viewed from the bottom side, the package pins start at the top row and go from the left edge to the right edge. Viewed from the top side, the pins start at the top row and go from the right edge to the left edge.

Product Availability

Table 25 - Table 27 show the planned packages and speed grades for XC4000-Series devices. Call your local sales office for the latest availability information, or see the Xilinx WEBLINX at http://www.xilinx.com for the latest revision of the specifications.

Table 25: Component Availability Chart for XC4000E FPGAs

	Speed Grade	PC 84	PQ 100	VQ 100	PG 120	TQ 144	PG 156	PQ 160	CB 164	PG 191	CB 196	PQ 208	HQ 208	PG 223	BG 225	CB 228	PQ 240	HQ 240	PG 299	HQ 304
XC 4003E	-4	C I	C I	C I	C I															
	-3	C	C	C	C															
	-2	C	C	C	C															
XC 4005E	-4	C I	C I			C I	C I M B	C I	M B			C I								
	-3	C	C			C	C	C				C								
	-2	C	C			C	C	C				C								
XC 4006E	-4	C I				C I	C I	C I				C I								
	-3	C				C	C	C				C								
	-2	C				C	C	C				C								
XC 4008E	-4	C I						C I		C I		C I								
	-3	C						C		C		C								
	-2	C						C		C		C								
XC 4010E	-4	C I						C I		C I MB	MB	C I	C I		C I					
	-3	C						C		C		C	C		C					
	-2	C						C		C		C	C		C					
XC 4013E	-4							C I				C I	C I	C I M B	C I	M B	C I	C I		
	-3							C				C	C	C	C		C	C		
	-2							C				C	C	C	C		C	C		
XC 4020E	-4												C I	C I				C I		
	-3												C	C				C		
	-2												C	C				C		
XC 4025E	-4													C I		M B		C I	C I M B	C I
	-3													C				C	C	C
	-2													C				C	C	C

C = Commercial, T_J = 0° to +85° C
I = Industrial, T_J = -40° to +100° C
M = Mil Temp, T_C = -55° to +125° C
B = MIL-STD-883C Class B, T_C = -55° to +125° C
Shaded device/package combinations are not supported.

Table 26: Component Availability Chart for XC4000EX FPGAs

	Speed Grade	HQ208	HQ240	PG299	HQ304	BG352	PG411	BG432
XC4028EX	-4	C I	C I	C I	C I	C I		
	-3	C	C	C	C	C		
XC4036EX	-4				C I		C I	C I
	-3				C		C	C
XC4044EX	-4						C I	C I
	-3						C	C

C = Commercial, T_J = 0° to +85° C
I = Industrial, T_J = -40° to +100° C
M = Mil Temp, T_C = -55° to +125° C
B = MIL-STD-883C Class B, T_C = -55° to +125° C
Shaded device/package combinations are not supported.

Table 27: Component Availability Chart for XC4000L and XC4000XL FPGAs

	Speed Grade	PC 84	TQ 176	PQ 208	HQ 208	BG 225	PQ 240	HQ 240	PG 299	HQ 304	BG 352	PG 411	BG 432	PG 475
XC4005L	-6	C		C										
	-5	C		C										
	-4													
XC4010L	-6	C	C	C										
	-5	C	C	C										
	-4													
XC4013L	-6			C		C	C							
	-5			C		C	C							
	-4													
XC4028XL					C			C	C	C	C			
XC4036XL										C		C	C	
XC4044XL												C	C	
XC4052XL												C	C	
XC4062XL														C

C = Commercial, T_J = 0° to +85° C
I = Industrial, T_J = -40° to +100° C
M = Mil Temp, T_C = -55° to +125° C
B = MIL-STD-883C Class B, T_C = -55° to +125° C
Shaded device/package combinations are not supported.
Speed grades for the XC4000XL have not yet been determined.

User I/O Per Package

Maximum available user I/O for each device/package combination is shown in Table 28 - Table 30.

Pinout tables for XC4000-Series devices follow. Pinout data is offered in two forms, as device-specific and package-specific tables. Device-specific tables include all packages for each XC4000-Series device. They follow the pad locations around the die, and include boundary scan register locations. Package-specific tables include all XC4000-Series devices available in a given package. These tables are especially useful in determining which pads should be avoided, in case of a future transition to a different device in the same package.

All pinouts defined at the time of publication are included in these tables. Additional information may be available. Call your local sales office or see the Xilinx WEBLINX at http://www.xilinx.com for the latest information.

Table 28: Maximum User I/O for XC4000E Device/Package Combinations

No. of Pins	Package (Code)	XC4003E	XC4005E	XC4006E	XC4008E	XC4010E	XC4013E	XC4020E	XC4025E
Maximum User I/O		**80**	**112**	**128**	**144**	**160**	**192**	**224**	**256**
84	PLCC (PC)	61	61	61	61	61			
100	PQFP (PQ)	77	77						
	VQFP (VQ)	77							
120	PGA (PG)	80							
144	TQFP (TQ)		112	113					
156	PGA (PG)		112	125					
160	PQFP (PQ)		112	128	129	129	129		
164	CBFP (CB)		112						
191	PGA (PG)				144	160			
196	CBFP (CB)					160			
208	PQFP (PQ)		112	128	144	160	160		
	HQFP (HQ)					160	160	160	
223	PGA (PG)						192	192	192
225	BGA (BG)					160	192		
228	CBFP (CB)						192		192
240	PQFP (PQ)						192		
	HQFP (HQ)						192	193	193
299	PGA (PG)								256
304	HQFP (HQ)								256

Note: This table includes standard user-programmable I/O. It also includes the TDI, TCK, and TMS pins, which can function as user-programmable I/O if not used for boundary scan. In addition to the I/O listed in this table, the M0 and M2 pins can be used as inputs only; the M1 and TDO pins can be used as outputs only. All of these pins must be called out using special library symbols. The XACT software does not use them by default. (See Table 18 on page 47.)

Table 29: Maximum User I/O for XC4000EX Device/Package Combinations

No. of Pins	Package (Code)	XC4028EX	XC4036EX	XC4044EX
Maximum User I/O		**256**	**288**	**320**
208	HQFP (HQ)	160		
240	HQFP (HQ)	193		
299	PGA (PG)	256		
304	HQFP (HQ)	256	256	
352	BGA (BG)	256		
411	PGA (PG)		288	320
432	BGA (BG)		288	320

Note: This table includes standard user-programmable I/O. It also includes the TDI, TCK. and TMS pins, which can function as user-programmable I/O if not used for boundary scan. In addition to the I/O listed in this table, the M0 and M2 pins can be used as inputs only; the M1 and TDO pins can be used as outputs only. All of these pins must be called out using special library symbols. The XACT software does not use them by default. (See Table 18 on page 47.)

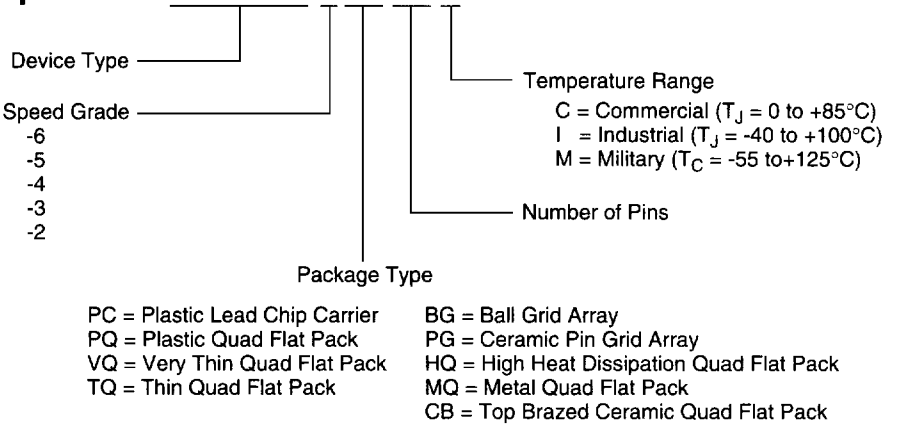
Table 30: Maximum User I/O for XC4000L and XC4000XL Device/Package Combinations

No. of Pins	Package (Code)	XC4005L	XC4010L	XC4013L	XC4028XL	XC4036XL	XC4044XL	XC4052XL	XC4062XL
Maximum User I/O		**112**	**160**	**192**	**256**	**288**	**320**	**352**	**384**
84	PLCC (PC)	61	61						
176	TQFP (TQ)		153						
208	PQFP (PQ)	112	160	160					
208	HQFP (HQ)				160				
225	BGA (BG)			192					
240	PQFP (PQ)			192					
240	HQFP (HQ)				193				
299	PGA (PG)				256				
304	HQFP (HQ)				256	256			
352	BGA (BG)				256				
411	PGA (PG)					288	320	352	
432	BGA (BG)					288	320	352	
475	PGA (PG)								384

Note: This table includes standard user-programmable I/O. It also includes the TDI, TCK, and TMS pins. which can function as user-programmable I/O if not used for boundary scan. In addition to the I/O listed in this table, the M0 and M2 pins can be used as inputs only; the M1 and TDO pins can be used as outputs only. All of these pins must be called out using special library symbols. The XACT software does not use them by default. (See Table 18 on page 47.)

Ordering Information

Example: **XC4013E-3HQ240C**



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